Operation and Service Manual

Precision Current Preamplifier

SIM918

Stanford Research Systems

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Certification

Stanford Research Systems certifies that this product met its published specifications at the time of shipment.

Warranty

This Stanford Research Systems product is warranted against defects in materials and workmanship for a period of one (1) year from the date of shipment.

Service

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Contents

General Information

The SIM918 Precision Current Preamplifier, part of Stanford Research Systems' Small Instrumentation Modules family, converts an input electric current into a proportional voltage output while maintaining zero potential difference between the input terminal and a bias terminal.

The main amplifier stage presents a transimpedance R_F, equal to the current gain of the preamplifier, to an input current i_{in}. The bias voltage V_{bias} is subtracted from the output of the stage, so that the voltage at the output of the instrument is

$$V_{out} = (V_{bias} - i_{in} \times R_F) - V_{bias} = -i_{in} \times R_F.$$

Safety and Preparation for Use

Connections

No dangerous voltages are generated by the module. However, the outer shield of the front-panel Input coaxial (BNC) connector in the SIM918 can be switched to the rear-panel Program input. If a dangerous voltage is applied to the Program terminal, it may be present on the outer shell of the Input connector, and may cause injury or death.

WARNING *Do not exceed* ±60 *volts to the Earth at the center terminal of the rear-panel Shield Program Voltage BNC connector.*

CAUTION *Do not exceed* ±15 *volts to the Earth at the center terminal of the front-panel Input and Bias BNC connectors, or at the center terminal of the rear-panel Ref Clock Sync BNC connector.*

Biomedical applications

WARNING Under certain conditions, the SIM918 may prove to be unsafe for applications involving human subjects. Incorrect grounding, component failure, and excessive common-mode input voltages are examples of conditions in which the instrument may expose the subject

to large input currents. Therefore, Stanford Research Systems does not recommend the SIM918 for such applications.

Caution regarding use with photomultipliers

⚠ CAUTION

The front-end amplifier of this instrument is easily damaged if a photomultiplier is used improperly with the preamplifier. When left completely unterminated, a cable connected to a PMT can charge to several hundred volts in a relatively short time. If this cable is connected to the curent input of the SIM918, the stored charge may damage the front-end JFET. To avoid this problem, provide a leakage path of about 100 kΩ to ground inside the base of the PMT to prevent charge accumulation.

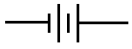
Service

Do not install substitute parts or perform unauthorized modifications to this instrument.

Preparation for use

The SIM918 is a single-wide module designed to be used inside the SIM900 Mainframe. Do not turn on the power to the mainframe or apply voltage or current inputs to the module until the module is completely inserted into the mainframe and locked in place.

Symbols you may Find on SRS Products

Symbol	Description
	Alternating current
	Caution - risk of electric shock
	Frame or chassis terminal
	Caution - refer to accompanying documents
	Earth (ground) terminal
	Battery
	Fuse
	On (supply)
	Off (supply)

Notation

The following notation will be used throughout this manual:

WARNING A warning means that injury or death is possible if the instructions are not obeyed.

CAUTION A caution means that damage to the instrument or other equipment is possible.

Typesetting conventions used in this manual are:

- Front-panel buttons are set as [GAIN ◄]; [GAIN ◄►] is shorthand for "[GAIN ◄] & [GAIN ►]".
- Front-panel indicators are set as *OVLD*.
- Signal names are set as ¬STATUS.
- Signal levels are set as HIGH.
- Remote command names are set as *IDN? .
- Literal text other than command names is set as `OFF`.
- Special ASCII characters are set as ⟨CR⟩.

Remote command examples will all be set in monospaced font. In these examples, data sent by the host computer to the SIM918 are set as `straight teletype font`, while responses received by the host computer from the SIM918 are set as *`slanted teletype font`*.

Specifications

Performance characteristics

		Min	Typ	Max	Units
Gain	Selection		10^6, 10^7, 10^8		V/A
	Accuracy, 10^6 V/A		±0.1		%
	10^7 V/A		±0.1		%
	10^8 V/A		±2		%
	Stability, 10^6 V/A		±10		ppm/°C
	10^7 V/A		±50		ppm/°C
	10^8 V/A		±100		ppm/°C
Current input	Selection		On, open		
	Offset voltage [1–3]			±10	μV
	Resistance			1	Ω
	Capacitance		18		pF
	Bias current, DC [3, 4]		1.0	3.0	pA
	AC [1, 4, 5]		3.5		pA rms
	Current noise at 100 Hz [6], 10^6 V/A		130		fA/$\sqrt{\text{Hz}}$
	10^7 V/A		42		fA/$\sqrt{\text{Hz}}$
	10^8 V/A		15		fA/$\sqrt{\text{Hz}}$
	Voltage noise [1, 5]		25		μV rms
	−3 dB bandwidth [6], 10^6 V/A		22		kHz
	10^7 V/A		12		kHz
	10^8 V/A		4		kHz
	Terminals		Isolated BNC [7]		
	BNC shield		Ground, bias, program /open		
Bias input	Selection		On, ground		
	Voltage [8]	−5.0		+5.0	V
	Resistance		10		MΩ
	−3 dB bandwidth		0.2		Hz
	Terminals		Isolated BNC [7]		
	BNC shield		Ground, float		
Program input	Voltage	−60		+60	V
	Resistance	3			GΩ
	Terminals		Grounded BNC [9], rear		
Reference clock sync	Selection		Input, output		
	Interface		Rear BNC [9], TTL [10]		
	Input frequency [11]	0.90		1.10	Hz
	Output frequency		1.0		Hz

		Min	Typ	Max	Units
Autozero	Selection	On, hold			
	Source	Internal, external reference clock			
	Switching frequency		0.50		Hz
Output	Voltage [8]	−10.0		+10.0	V
	Maximum current	±100			mA
	Short circuit duration	Indefinite			
	Resistance		100		Ω
	Offset voltage [2]			±50	μV
	Common-mode rejection, DC	80			dB
	Terminals	Grounded BNC [7]			
Operating	Temperature [12]	0		40	°C
	Power	+5, ±15			V DC
	Supply current, +5 V		100		mA
	±15 V		150		mA

Conditions:

[1] With autozero on.
[2] Following an autocalibration at (23 ± 5) °C within 24 hours.
[3] 100 s average.
[4] At 23 °C. Doubles every 6 °C to 10 °C.
[5] 0.1 Hz to 10 Hz.
[6] For a 100 pF source capacitance and an infinite source resistance. Higher values of source capacitance or a finite source resistance will degrade these specifications.
[7] Amphenol 31–10–4052 or similar.
[8] An overload will be detected and the instrument is not guaranteed to perform properly if these limits are exceeded, or if $|V_{\text{bias}} - i_{\text{in}} \times R_{\text{F}}|$ exceeds the limits. Continuous application of a bias voltage V_{bias} in excess of ±15 V will damage the instrument.
[9] Tyco 227169–4 or similar.
[10] Rising-edge sensitive.
[11] External reference clock capture range. The instrument is not guaranteed to perform properly if these limits are exceeded.
[12] Non-condensing.

General characteristics

Interface	Serial (RS–232) through SIM interface
Connectors	BNC (3 front [7], 2 rear [9]); DB–15 (male) SIM interface
Weight	1.7 lbs
Dimensions	1.5″ W × 3.6″ H × 7.0″ D

1 Getting Started

This chapter gives you the necessary information to get started quickly with your SIM918 Precision Current Preamplifier.

In This Chapter

1.1 Introduction to the Instrument

1.1.1 Current amplifiers and autozero

A current, or transimpedance, amplifier converts electric current into a proportional output voltage. Unlike a simple resistor, the amplifier presents a low-impedance terminal to the input current. In the SIM918 Precision Current Preamplifier, the electric potential of the input terminal, V_{in}, is accurately made equal to the user-provided potential at the bias terminal, V_{bias}, or to ground. The absolute magnitude of the resulting input *offset voltage* is nearly zero:

offset voltage

$$V_{\text{ofs}} = V_{\text{in}} - V_{\text{bias}}, \qquad |V_{\text{ofs}}| < 10\,\mu\text{V}.$$

In all transimpedance amplifiers, the input potential is kept near that of the bias through the action of negative feedback. When the bias voltage is at ground, the input terminal is often said to present a virtual ground, or a virtual null. Without autozeroing, this virtual ground drifts, in some cases by many millivolts. This error in the electric potential of the input terminal may be unacceptable in precision measurements.

virtual ground

In the SIM918, an autozero circuit measures V_{ofs} every 2 seconds and makes the adjustment necessary to keep the offset voltage at zero. The autozero feature can be engaged or inhibited remotely or from the front panel, giving the user flexibility in sensitive applications. With autozero inhibited, the preamplifier retains microvolt input accuracy for many hours. When engaged, it takes the autozero only a few cycles of a reference clock to restore the offset to within its specified limits.

The gain, or transimpedance, of the preamplifier can be set to $R_{\text{F}} = 10^6$, 10^7, or 10^8 V/A, remotely and from the front panel. Along with voltage accuracy, the SIM918 offers a low input bias current[1] and a current noise that is close to the lower limit imposed by the Johnson noise of the transimpedance.

1.1.2 Clocks

The autozero circuit switches between measuring the input offset voltage, and the offset voltage of the zeroing amplifier itself, at one half the frequency of an internal or external *reference clock*. The internal clock signal (typically 1.0 pulse per second, *pps*, i.e. 1.0 Hz) can be selected, remotely or from the front panel, to be output on

reference clock
one pps

[1] In the unfortunate but established terminology of electronics, the word *bias* conveys different meanings. The *bias current* is the input current present in the instrument in the absence of a current from an external source.

a rear-panel connector. Alternatively, the same connector can be used to input a clock signal at (1.0 ± 10%) pps (i.e. 1.10 Hz–0.90 Hz), synchronizing the switching to an external source.

The reference clock in the SIM918 operates independently of the oscillator used to clock the digital control circuitry. The latter is designed with a special clock-stopping architecture. The microcontroller is turned on only in the following cases: when the settings are being changed; autozero is turned on or off; and during autocalibration, remote communications, or when an overload condition or an external reference clock event occurs. This guarantees that no digital noise contaminates low-level analog signals.

With autozero off and in the absense of an external clock input, the preamplifier enters a completely quiescent state: no reference clock transitions are present that can disturb the measurement of a low-level electric current.

1.1.3 Cabling and grounding

The SIM918 provides maximum flexibility for cabling and grounding. The input connection can be opened, and the bias voltage can be connected to signal ground.

The shield of the Input BNC can be switched between signal ground, the bias voltage, or the rear-panel Program input (which can be left floating, if desired). With the Program input, a user can supply an excitation potential to an experiment via the shield conductor of the input cable, while the excited current flows through the center conductor to the SIM918. The shield of the Bias BNC can be independently grounded or floated.

The input and bias selections, and those of their shields, can be made via the push of a front-panel button or remotely.

1.1.4 Autocalibration

A user-commanded autocalibration procedure allows one to eliminate the effects of thermal drifts in the autozero circuit, and to reduce output offset voltage.

1.1.5 Remote interface and status

remote interface

A remote computer can access the module through the SIM900 Mainframe, using RS–232 or GPIB. All instrument settings can be queried via the remote interface. The SIM918 can be operated outside the SIM900 Mainframe by powering it with its required DC voltages.

If the maximum bias voltage is exceeded, or the chosen gain setting causes the output voltage to exceed its maximum, the appropriate overload LED turns on. If the module cannot lock to an external reference clock signal, an LED indicates an unlocked state. If armed, the module also generates a status signal to alert the user of the overload or unlocked condition.

1.1.6 Block diagram

The output of the main amplifier (transimpedance stage) is referenced to the bias voltage. A difference amplifier subtracts the bias voltage, so the output of the instrument is directly proportional to the input current i_{in} and the gain R_{F}:

$$V_{\text{out}} = (V_{\text{bias}} - i_{\text{in}} \times R_{\text{F}}) - V_{\text{bias}} = -i_{\text{in}} \times R_{\text{F}}. \tag{1.1}$$

A block diagram of the preamplifier is shown below in Figure 1.1.

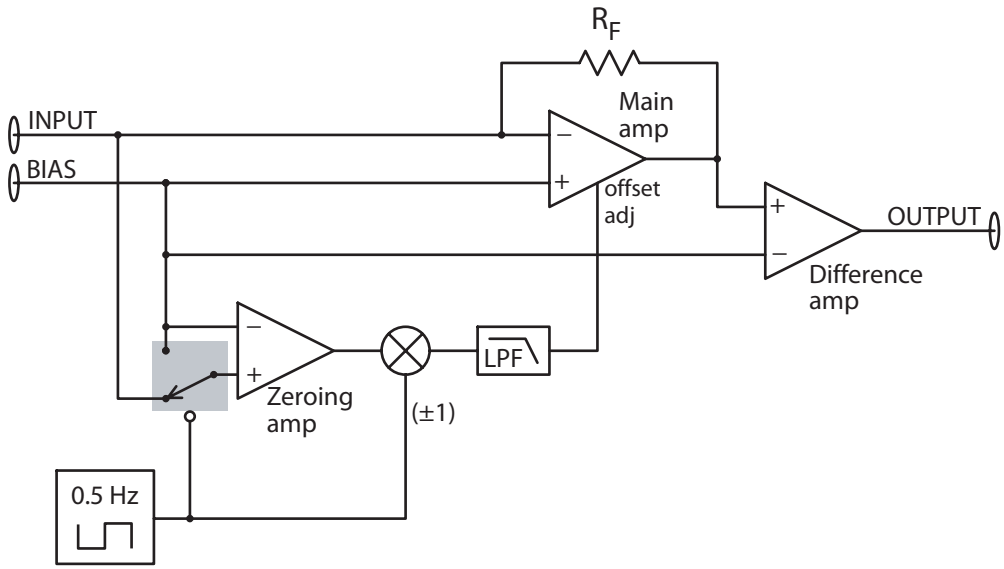


Figure 1.1: The SIM918 block diagram.

1.1.7 Front and rear panels

Figure 1.2: The SIM918 front and rear panels.

1.2 Front-Panel Operation

1.2.1 Gain

The gain R_F of the preamplifier, in volts per microampere, is indicated on the front panel of the instrument via a green annunciator LED.[2] Press one of the [GAIN ◄►] buttons to change the gain. If [GAIN ◄] is pressed when $R_F = 1\,V/\mu A$, the press has no effect. If [GAIN ►] is pressed when $R_F = 100\,V/\mu A$, the press has no effect.

A simultaneous press of [GAIN ◄►] has a special meaning. This press initiates autocalibration (Section 2.6).

1.2.2 Autozero

1.2.2.1 Engaging the autozero circuit

The autozero circuit is turned *ON* by the press of a front-panel button. There will be a pause of up to 3.3 seconds (a wait for a positive-going edge of the reference clock). At the end of the pause, the green

[2] Note the minus sign in Eq. (1.1); the output voltage is positive for a current that flows *out of* the input terminal.

annunciator LED will turn on and the zeroing circuit will become active.

The same button turns autozeroing off. There will be a less than 1 s pause in order for the present control output of the autozero circuit to be sampled and stored. At the end of the pause, the LED indicator will turn off and all switching inside the SIM918 will cease. The sampled control output (trim) will remain applied to the transimpedance-stage amplifier, zeroing it to the best of precision available at the time the autozero circuitry is inhibited.

1.2.2.2 Reference clock detection

The autozero circuit switches at one half the frequency of an internal or external reference clock. If a periodic TTL-level signal is applied to the rear-panel Ref Clock Sync connector, and the connector is not selected for output (see the next section), the preamplifier will recognize the external clock and attempt to lock to the signal. The green *External* LED will illuminate for the duration of the external clock input.

capture range
lock acquisition time

If the frequency of the external clock is stable and is between 0.90 Hz and 1.10 Hz, the module will successfully lock to the signal. It typically takes 250 s (just over 4 minutes) to acquire a lock. The yellow *Unlocked* LED is illuminated whenever the SIM918 is not in a locked state. For further discussion of locking, see Chapter 2.5.

For the duration of an unlocked state, the switches in the autozero circuit are not guaranteed to have correct duty cycles. Therefore, the specified input offset accuracy is not guaranteed while *Unlocked*.

The internal reference clock is used when an external clock signal is not present. In this state, neither the *External* LED nor the *Unlocked* LED is illuminated.

1.2.2.3 Output 1 pps sync

The rear-panel Ref Clock Sync connector can be used to output the internal reference clock. The signal at the output is TTL, typically at 1.0 Hz (1.0 pps). The [Output 1 pps sync] button toggles the direction of the signal at the rear-panel connector. The output direction is indicated by a green LED. An inactive *Output 1 pps sync* indicates that the connector may be used to input an external clock.

If [Output 1 pps sync] is pressed while an external reference clock signal is present at the connector, clock output will fail and a Device-Dependent Error (Section 3.5.3) will be issued. If an external signal is applied to the Ref Clock Sync terminal while the connector is selected for output, the external signal will not be recognized.

1.2.3 Input

The [INPUT Open] button opens and closes a relay in the path of the input current. A green LED indicates a disconnected input terminal. The input capacitance of the SIM918 is at its lowest with input open, and is specified in the table on Page viii.

1.2.3.1 Input shield

Successive presses of the [INPUT Shield] button connect the outer shell of the Input BNC to the rear-panel Shield Program Voltage terminal, a buffered copy of the bias voltage, and to signal ground. The state of the input shield connection is indicated by one of three LEDs: the yellow *INPUT Shield Prog*, the yellow *INPUT Shield Bias*, or the green *INPUT Shield GND*.

To float the shield of the Input connector, leave the Shield Program Voltage BNC open and select *INPUT Shield Prog*.

1.2.4 Bias

The [BIAS GND] button toggles the source of the bias between the voltage at the center terminal of the Bias BNC and the signal ground of the instrument. If the bias source is set to ground, the green *BIAS GND* light is on.

With Bias grounded, the difference amplifier (Figure 1.1) is switched out and the output of the instrument is taken directly from the transimpedance stage. With this configuration, there is no common-mode error and the output-offset error is reduced.

When Bias is connected to a user voltage, the voltage is buffered internally before being distributed to other parts of the preamplifier. The offset error of the bias buffer is included in the input offset accuracy specifications in the table on Page viii.

1.2.4.1 Bias overload

bias overload limits

An overload condition is recognized and the *BIAS OVLD* LED is activated if the absolute value of the voltage applied to the Bias input exceeds certain limits. These limits are typically ±5.0 V, and are between

$$-5.2\,\mathrm{V} \le V_{\mathrm{min}} \le -4.9\,\mathrm{V}, \quad 4.9\,\mathrm{V} \le V_{\mathrm{max}} \le 5.2\,\mathrm{V}.$$

The overload LED stays on for a minimum of 50 ms; after this time it turns off if the overload condition has ceased.

1.2.4.2 Bias shield

Successive presses of the [BIAS Shield] button float the outer shell of the Bias BNC and connect it to ground. The state of the bias shield connection is indicated by one of two LEDs: the yellow *BIAS Shield Float* or the green *BIAS Shield GND*.

Note that it is the electric *potential* at the Bias terminal, not the potential difference across the Bias connector, that the autozero circuit uses as the reference for the input voltage.

1.2.5 Output overload

output overload limits

An overload condition is recognized and the *OUTPUT OVLD* LED is activated if the absolute value $|i_{\text{in}} \times R_{\text{F}}|$ exceeds certain limits. These limits are typically ±10.0 V, and are between

$$-10.4\,\text{V} \le V_{\text{min}} \le -9.9\,\text{V}, \quad 9.9\,\text{V} \le V_{\text{max}} \le 10.4\,\text{V}.$$

The overloaded state is also recognized, and *OUTPUT OVLD* activated, if the raw output of the transimpedance stage, $|V_{\text{bias}} - i_{\text{in}} \times R_{\text{F}}|$, exceeds these limits. To distinguish between the two output overload possibilities, use the OVLD? query. The overload LED stays on for a minimum of 50 ms; after this time it turns off if the overload condition has ceased.

1.3 Connections

There are five BNC connectors in the SIM918, three on the front panel and two at the rear.

Panel	BNC	Terminal	Signal	Direction
Front	Input	Center	Input current	Input
		Shield	Shield program voltage, bias voltage, signal ground	Output
	Bias	Center	Bias voltage	Input
		Shield	Float, power ground	
	Output	Center	Output voltage	Output
		Shield	Signal ground	Output
Rear	Shield Program Voltage	Center	Shield program voltage	Input
		Shield	Chassis ground	
	Ref Clock Sync	Center	Reference clock	Input, output
		Shield	Chassis ground	Input, output

Table 1.1: BNC connections in the SIM918.

For a further discussion of grounding, see Section 2.2.1. The SIM interface connector is discussed in Section 1.6.1.

1.4 Power-On

The instrument retains the following settings in non-volatile memory:

1. The power line frequency (FPLC): 60 Hz or 50 Hz.[3]
2. The gain.
3. Autozero on/off.
4. Input selection (on, open).
5. Input shield selection (program, bias, ground.)
6. Bias selection (on, ground).
7. Bias shield selection (float, ground.)
8. Whether or not the phase-locked loop (Section 2.5) stays active when autozero is off.
9. Calibration values.

The power-on configuration of the remote interface is detailed in Section 3.3.1.

1.5 Restoring the Default Configuration

The default configuration of the SIM918 is:

1. Gain 10^6 V/A.
2. Autozero on.
3. Input connected.
4. Input shield at ground.
5. Bias at ground.
6. Bias shield at ground.
7. Reference clock direction is input.
8. The phase-locked loop (Section 2.5) is inactive when autozero is off.

To reset the module into this configuration, turn the SIM900 Mainframe power on while holding a front-panel button of the SIM918 for at least 2.0 seconds. The same configuration can also be reached from the remote interface by issuing the *RST command.

[3] FPLC equals the principal rejection frequency of an internal analog-to-digital converter used to measure the input offset trim. See the command OFST.

1.6 SIM Interface

The primary connection to the SIM918 Precision Current Preamplifier is the rear-panel DB–15 SIM interface connector. Typically, the SIM918 is mated to a SIM900 Mainframe via this connection, either through one of the internal mainframe slots or the remote cable interface.

It is also possible to operate the SIM918 directly, without using the SIM900 Mainframe. This section provides details on the interface.

1.6.1 SIM interface connector

The DB–15 SIM interface connector carries all the power and communication lines to the instrument. The connector signals are specified in Table 1.2.

Pin	Signal	Direction Src ⇒ Dest	Description
1	SIGNAL_GND	MF ⇒ SIM	Signal ground
2	¬STATUS	SIM ⇒ MF	Status/service request (GND = asserted, +5 V= idle)
3	RTS	MF ⇒ SIM	HW handshake (unused in SIM918)
4	CTS	SIM ⇒ MF	HW handshake (unused in SIM918)
5	¬REF_10MHZ	MF ⇒ SIM	10 MHz reference (no connection in SIM918)
6	−5V	MF ⇒ SIM	Power supply (no connection in SIM918)
7	−15V	MF ⇒ SIM	Power supply
8	PS_RTN	MF ⇒ SIM	Power ground
9	CHASSIS_GND		Chassis ground
10	TXD	MF ⇒ SIM	Async data (start bit = "0"= +5 V; "1" = GND)
11	RXD	SIM ⇒ MF	Async data (start bit = "0"= +5 V; "1" = GND)
12	REF_10MHZ	MF ⇒ SIM	10 MHz reference (no connection in SIM918)
13	+5V	MF ⇒ SIM	Power supply
14	+15V	MF ⇒ SIM	Power supply
15	+24V	MF ⇒ SIM	Power supply (no connection in SIM918)

Table 1.2: SIM interface connector pin assignments, DB–15.

1.6.2 Direct interfacing

The SIM918 is intended for operation in the SIM900 Mainframe, but users may wish to directly interface the module to their own systems without the use of additional hardware.

The mating connector needed is a standard DB–15 receptacle, such as Tyco part number 747909–2 (or equivalent). Clean, well-regulated supply voltages of ±15.0 V DC, +5.0 V DC must be provided, following the pinout specified in Table 1.2 and the minimum currents in the table on Page ix. Ground must be provided on Pins 1 and 8, with chassis ground on Pin 9. The ¬STATUS signal may be monitored

on Pin 2 for a low-going TTL-compatible output indicating a status message. See Section 3.5 for the description of status messages.

⚠ CAUTION

The SIM918 has no internal protection against reverse polarity, missing supply, or overvoltage on the +5 *V and the* ±15 *V power-supply pins. Supply voltages above* 5.5 *V on Pin 13, above* +16 *V on Pin 14, or below* −16 *V on Pin 7 are likely to damage the instrument. SRS recommends using the SIM918 together with the SIM900 Mainframe for most applications.*

1.6.2.1 Direct interface cabling

If the user intends to directly wire the SIM918 independent of the SIM900 Mainframe, communication is usually possible by directly connecting the appropriate interface lines from the SIM918 DB–15 plug to the RS–232 serial port of a personal computer.[4] Connect RXD from the SIM918 directly to RxD on the PC, TXD directly to TxD. In other words, a null-modem-style cable is *not* needed.

To interface directly to the DB–9 male (DTE) RS–232 port typically found on contemporary personal computers, a cable must be made with a female DB–15 socket to mate with the SIM918, and a female DB–9 socket to mate with the PC's serial port. Separate leads from the DB–15 need to go to the power supply, making what is sometimes know as a "hydra" cable. The pin connections are given in Table 1.3.

DB–15/F to SIM918		Name
	DB–9/F	
10 ⟷	3	TxD
11 ⟷	2	RxD
	5	Computer Ground
	to Power Supply	
7 ⟷	−15 V DC	
13 ⟷	+5 V DC	
14 ⟷	+15 V DC	
1 ⟷	Signal Ground (separate wire to Ground)	
8 ⟷	Power Ground (separate wire to Ground)	
9 ⟷	Chassis Ground (separate wire to Ground)	

Table 1.3: SIM918 direct interface cable pin assignments.

note about grounds

The distinct Signal Ground and Power Ground, and the chassis ground, are *not* directly connected within the SIM918. The power

[4] Although the serial interface lines on the DB–15 do not satisfy the minimum voltage levels of the RS–232 standard, these lines are typically compatible with desktop personal computers.

ground carries the return currents of digital control signals, power-intensive analog amplifiers, and the power supplies, whereas the output voltage references to a stable signal ground (Section 2.2.1). When operating in the SIM900, the three grounds are tied together in the SIM900 Mainframe. Signal Ground and Power Ground are connected through back-to-back Schottky diodes, so they cannot be more than ~ ±0.35 V apart. The three ground lines should be separately wired to a single, low-impedance ground source at the power supply.

1.6.2.2 Serial settings

The initial serial port settings at power-on are: baud rate 9600, 8 bits, no parity, 1 stop bit, and no flow control. The baud rate of the SIM918 cannot be changed. Flow control is not implemented in the SIM918. The parity may be changed with the PARI command.

2 Description of Operation

This chapter provides a number of additional details of the operation of the SIM918.

In This Chapter

2.1 About Transimpedance Amplifiers

transimpedance amplifier

A *transimpedance amplifier* is an operational amplifier with a resistor in the feedback path. More generally, the feedback impedance Z_F always has a resistive and a reactive component. The two inputs to the operational amplifier have a very high impedance; and the feedback in the amplifier acts to keep the two inputs at the same electric potential. Therefore, the input current i_{in} is forced through the feedback impedance, and the amplifier produces an output voltage

$$V_{out,\,TA} = V_{bias} - i_{in} \times Z_F.$$

The amplifier acts to translate the input current into a proportional output voltage, with the feedback impedance being the coefficient of proportionality. Hence the term *transimpedance*.

The main amplifier of the SIM918 Precision Current Preamplifier is a transimpedance amplifier based on a composite, JFET-input design.

2.1.1 Input capacitance and stability

The input impedance of JFET devices is extremely large. However, the impedance experienced, as a whole, by a current input to the feedback amplifier (i.e. the change in the input voltage[1] divided by the input current) has two other, much more significant contributions in parallel. The first one is the effect of the output on the input via feedback due to finite open-loop voltage gain of the operational amplifier, and the second one is input capacitance.

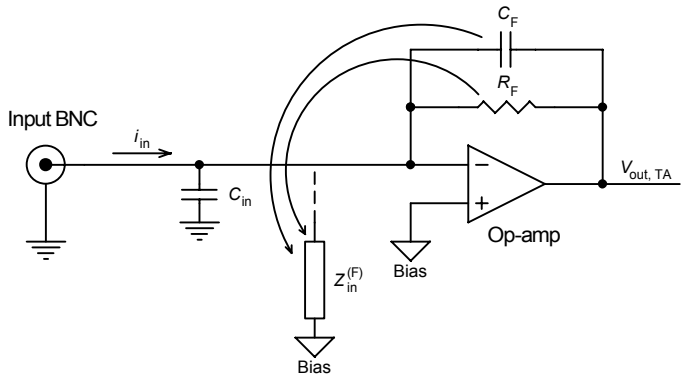


Figure 2.1: A transimpedance amplifier.

The first term equals the feedback impedance divided by the open-loop gain of the operational amplifier[2]:

$$Z_{in}^{(F)} = Z_F / A_{OL} \tag{2.1}$$

[1] Without the action of the autozero circuit.
[2] Within the current bandwidth of the transimpedance amplifier.

and is below 1 Ω at DC. The open-loop gain is very high at DC, and typically decreases as inverse frequency with a corresponding 90° phase lag:

$$A_{OL} = -j\, f_T/f$$

where f_T is the gain-bandwidth product of the operational amplifier (~ 10 MHz in the SIM918). Substituting into Equation (2.1), observe

$$Z_{in}^{(F)} = j\, \frac{Z_F}{f_T}\, f.$$

If the feedback element is purely resistive, the term due to Z_F behaves exactly as if a large inductor were connected between the input and the bias terminals. This contribution to the input impedance increases linearly with frequency, with a corresponding 90° phase lead.[3]

The input terminal always has some amount of parasitic capacitance to the bias terminal, and to ground. The input capacitance specification in the table on Page viii applies for no cable connected to the Input BNC. A coaxial cable adds ~ 100 pF/m of capacitance. Even one meter of coax will dramatically increase the input capacitance.

The input capacitance, in parallel with the effective inductance, can form a resonant tank circuit if the capacitance is large enough that the resulting resonant frequency lies within the bandwidth of the transimpedance amplifier. The SIM918 has adequate compensation (feedback capacitance) to prevent oscillation for up to 100 pF of additional input capacitance.[4] To avoid a feedback oscillation, follow these steps:

1. Place the preamplifier as close as possible to the signal being measured, and use the shortest cable length necessary to connect them.
2. Reduce all stray capacitance to bias or ground at the output of the experiment under measurement.
3. Use a lower gain setting, which reduces the effective input inductance.

Other detrimental effects of excess input capacitance include reduced current bandwidth, poor step response (overshoot and ringing), and increased output noise.

2.1.2 Choosing the right gain

It is important to consider the output resistance (in general, impedance) of the current source being measured. The transimpedance

[3] The input voltage leads the input current.
[4] Longer cable lengths are tolerated at lower gain settings.

stage amplifies its input voltage noise by the factor[5] of $(1+R_F/R_{source})$, where R_{source} is the source resistance. This noise adds in quadrature with the current noise of the stage.To prevent the voltage noise term from dominating the overall output noise, set the current gain to

$$R_F \lesssim R_{source}.$$

2.2 Bias and Ground

2.2.1 Grounds

The output of the SIM918 is referenced to ground. To maintain the DC accuracy of the instrument, there are two separate ground references. Power Ground (Pin 8 of the SIM interface connector) provides a current return path for digital control signals, power-intensive analog amplifiers, and the power supplies. Signal Ground (Pin 1 of the interface connector) serves as the reference point for analog voltages. The outer shell of the Output BNC connector is tied to Signal Ground. The output current of the preamplifier returns to the power supply through Signal Ground. When *INPUT Shield GND* is selected, the shell of the Input BNC is also tied to Signal Ground.

The outer shells of the rear-panel Shield Program Voltage and Ref Clock Sync BNCs are connected to chassis ground, Pin 9 of the DB–15 SIM interface connector. The separate power, signal, and chassis grounds are *not* directly connected within the preamplifier. When operating in the SIM900 Mainframe, the three grounds are tied together inside the mainframe, and through the mainframe to the Earth. The signal and power grounds are connected inside the SIM918 through back-to-back Schottky diodes, so they cannot be more than ~ ±0.35 V apart.

2.2.2 Bias

The bias potential is received by an ultralow-offset voltage buffer. It is this buffered voltage that appears on the shield of the Input BNC when *INPUT Shield Bias* is selected.

The shield of the Bias connector is not used as a reference for the bias voltage. When *Bias Shield GND* is selected, the shield is at Signal Ground. The limits on the bias voltage in Section 1.2.4.1 are relative to this ground. A voltage exceeding these limits by more than 1 V will be clamped , through diodes, to ±5.5 V relative to Power Ground. The 10 MΩ input resistor is connected between Bias and Signal Ground.

[5] At frequencies low enough that the resistive components of the two impedances are dominant.

To reduce output noise of the SIM918, the Bias input is limited to a bandwidth specified in the table on Page viii. Beyond this frequency, the transimpedance stage cannot follow variations in the bias voltage, but the output difference amplifier (discussed in the next section) does. Hence the common-mode rejection of the instrument is greatly reduced at frequencies above DC.

The bias sensing circuitry is always active, and will signal *BIAS OVLD* when the applied input exceeds the voltage limits in Section 1.2.4.1, even if Bias is set to *GND*.

2.3 Output

When Bias is switched to *GND*, the output of the instrument is taken directly from the transimpedance stage; otherwise, from a difference amplifier (Figure 1.1) that subtracts the bias voltage from the output of the transimpedance stage. Both outputs have equal drive capacity.

The output impedance of the SIM918 Precision Current Preamplifier is 100 Ω. The preamplifier can drive load impedances from ∞ to 0 Ω for the full ±10 V range of output voltage. When driving a 50 Ω load, the gain will be one third of that displayed on the front panel.

The output signal is filtered by a passive LRC, with $f_{-3\,\mathrm{dB}} = 25\,\mathrm{kHz}$. The filter eliminates broad-spectrum noise, while adding a negligible amount of overshoot in the step response. The *R* in the filter contributes to the output resistance.

The output difference amplifier, when engaged (Bias not at [GND]), introduces an offset error that can be greater than the maximum input offset error of the preamplifier. The error is reduced by autocalibration (Section 2.6). The output offset can also be trimmed from the remote interface by using the command OFST 1.

2.4 Autozero Trim

The autozero control loop is fully analog.[6] Its settling time, to within the maximum input offset voltage specification in the table on Page viii, is 40 s. Two adjustments can be made to loop parameters via the remote command OFST. The first one to consider, OFST 3, adjusts the zero point of the loop itself, i.e. the voltage to which the control loop drives the input offset when autozero is *ON*.

The command OFST 2 sets the code in a digital-to-analog converter, the output of which adds together with the output of the loop to form the overall control output of the autozero circuit. When autozero is engaged, the control loop will compensate for changes made

[6] With discrete time steps.

via OFST 2, driving the input offset voltage back to a value determined by OFST 3. With autozero off, OFST 3 has no effect and OFST 2 changes the input offset directly.

The best value for OFST 2 is readjusted each time autozero is turned from on to off. If the preamplifier is to be operated under conditions that tolerate absolutely no clock transitions, the recommended course of action is to turn autozero on, let the control loop drive the output to zero and settle, and turn autozero off for the duration of the experiment (Section 2.8).

The value for OFST 3 is reestablished by autocalibration (Section 2.6).

2.5 Phase-Locked Loop

The switches in the autozero circuit receive a clock signal from an internal phase-locked loop. If an external reference clock is available at the rear-panel Ref Clock Sync connector, autozero is on, and the connector is not selected for output, the PLL will attempt to lock to the clock signal. The synchronization will be successful for external clock frequencies between 0.90 Hz and 1.10 Hz.

In the internal reference clock mode, the PLL oscillator runs freely, generating a 1.0 Hz square wave with rising edges at the beginning of each autozero half-cycle. The voltage-controlled oscillator in the loop operates at 240 Hz for 60 Hz power line frequency (FPLC), and at 200 Hz for FPLC = 50 Hz.

The PLL can be automatically inhibited, and the voltage-controlled oscillator turned off, when the reference clock is *External* and autozero is off. The behavior is set by the remote command APLL. With APLL OFF, the oscillator turns off. In this mode, under external reference clock, the instrument will undergo the full capture and lock transient after autozero is switched on. To avoid the 4 minute capture delay, set APLL ON. The module restores the last known APLL mode upon power-on.

When autozero is on, the PLL oscillator is always running, regardless of the reference clock source. If the reference clock is internal and autozero is off, the PLL oscillator is off. There is no capture delay under internal clock.

2.6 Autocalibration

To ensure the specified offset accuracy, the preamplifier must be self-calibrated within the 24 hours preceding a measurement. A valid autocalibration must take place at (23 ± 5) °C with the module warmed up for at least 2 hours at (23 ± 5) °C. If the module is being used inside

the SIM900 Mainframe, the autocalibration must also be inside the mainframe. Otherwise, perform the autocalibration with the same connection to an independent supply as you use for the operation.

Disconnect all inputs and outputs to the SIM918 while performing the autocalibration. Connect the center and shield terminals of the Bias BNC together externally, e.g. with a grounding cap. To calibrate, issue the command ACAL, or press both [GAIN ◄►] at the same time. Depending on the firmware revision, *the calibration may take up to 20 minutes to complete.* During the autocalibration, all LEDs are lit. At the end of the calibration, the module returns to its pre-ACAL settings, except the reference clock direction is reset to input.

If autocalibration is unsuccessful, for example because an external current is applied to Input, the calibration constants revert to their original values and the command LDDE? will return Code 2. If an external reference clock is detected, the autocalibration terminates immediately with LDDE? 2.

Autocalibration does not affect gain accuracy.

2.7 Clock Stopping

The microprocessor clock of the SIM918 stops if the module is idle, "freezing" the digital circuitry. The following actions "wake up" the clock:

1. A power-on.
2. A press of a front-panel button.
3. Activity (send or receive) at the remote interface.
4. An overload.
5. A change in external reference clock status: several rising edges at the rear-panel connector while in internal clock mode, or cessation of clocking while in external mode.
6. Loss of PLL lock.

The clock runs for as long as is necessary to complete a change of settings requested from the front panel, or to communicate the output of a query through the remote interface. However, the clock will remain active for as long as the overload or unlocked condition exists, and for the full duration of an autocalibration.

This default behavior can be modified with the remote command AWAK. Setting AWAK ON will prevent the clock from stopping. The module returns to AWAK OFF upon power-on.

Note that the operation of the PLL oscillator is completely independent of the microprocessor clock.

2.8 Quiescent Operation

Follow these steps to operate the SIM918 Precision Current Preamplifier in sensitive measurements that can tolerate absolutely no module clock transitions:

1. Reset the preamplifier (Section 1.5).
2. Set Input to *Open*.
3. Wait for at least 40 s.
4. Turn autozero off.
5. Select the desired gain.
6. Close the input.
7. Perform the measurement.

After this sequence is complete, the control output of the autozero circuit holds at a value that initially drives the input offset within its specification. Without active autozeroing, the input offset may drift as time progresses, so Steps 1–6 may need to be repeated.

3 Remote Operation

This chapter describes operating the SIM918 over the serial interface.

In This Chapter

3.1 Index of Common Commands

Symbol	Definition
i	Bit number (0–7)
j	Unsigned integer (0–65535)
m	Unsigned integer (1–3)
y, z	Literal token
(?)	Required for queries; illegal for set commands
var	Parameter always required
{*var*}	Required parameter for set commands; illegal for queries
[*var*]	Optional parameter for both set and query forms

Interface

Serial Communications

3.2 Alphabetic List of Commands

3.3 Introduction

Remote operation of the SIM918 is through a simple command language documented in this chapter. Both set and query forms of most commands are supported, allowing the user complete control of the amplifier from a remote computer, either through the SIM900 Mainframe or directly via RS–232 (see Section 1.6.2.1).

See Table 1.2 for the specification of the DB–15 SIM Interface Connector.

3.3.1 Power-on configuration

The initial settings for the remote interface are 9600 baud with no parity and no flow control, and with local echo disabled (CONS `OFF`).

The following values are retained in non-volatile memory:

1. The power line frequency (FPLC).
2. The gain.
3. Autozero on/off.
4. Input selection (on, open).
5. Input shield selection (program, bias, ground.)
6. Bias selection (on, ground).
7. Bias shield selection (float, ground.)
8. Whether or not the phase-locked loop stays active when autozero is off.
9. Calibration values.

Upon power-on, those settings are restored to their values before the power was turned off.

Where appropriate, the default or power-on value for parameters is listed in **`boldface`** in the command descriptions.

3.3.2 Buffers

The SIM918 stores incoming bytes from the host interface in a 64-byte input buffer. Characters accumulate in the input buffer until a command terminator (either ⟨CR⟩ or ⟨LF⟩) is received, at which point the message is parsed and executed. Query responses from the SIM918 are buffered in a 64-byte output queue.

If the input buffer overflows, then all data in *both* the input buffer and the output queue are discarded, and an error is recorded in the CESR and ESR status registers.

3.3.3 Device Clear

The SIM918 host interface can be asynchronously reset to its power-on configuration by sending an RS–232-style ⟨break⟩ signal. From the SIM900 Mainframe, this is accomplished with the SRST command; if directly interfacing via RS–232, then use a serial break signal. After receiving the Device Clear, the CONS mode is turned OFF. Note that this *only* resets the communication interface; the basic function of the SIM918 is left unchanged; to reset the preamplifier, use *RST.

The Device Clear signal will also terminate the output of the HELP? command from the SIM918.

3.4 Commands

This section provides syntax and operational descriptions for remote commands.

3.4.1 Command syntax

The four letter mnemonic (shown in CAPS) in each command sequence specifies the command. The rest of the sequence consists of parameters.

Commands may take either *set* or *query* form, depending on whether the "?" character follows the mnemonic. *Set only* commands are listed without the "?", *query only* commands show the "?" after the mnemonic, and *optionally query* commands are marked with a "(?)".

Parameters shown in { } and [ ] are not always required. Parameters in { } are required to set a value, and should be omitted for queries. Parameters in [ ] are optional in both set and query commands. Parameters listed without surrounding characters are always required.

Do *not* send ( ) or { } or [ ] as part of the command.

Multiple parameters are separated by commas. Multiple commands may be sent on one command line by separating them with semicolons (;) so long as the input buffer does not overflow. Commands are terminated by either ⟨CR⟩ or ⟨LF⟩ characters. Null commands and whitespaces are ignored. Execution of the command does not begin until the command terminator is received.

tokens *Token* parameters (generically shown as *y* and *z* in the command descriptions) can be specified either as a keyword or as an integer

value. Command descriptions list the valid keyword options, with each keyword followed by its corresponding integer value. For example, to set the response termination sequence to ⟨CR⟩+⟨LF⟩, the following two commands are equivalent:

TERM CRLF —or— TERM 3

For queries that return token values, the return format (keyword or integer) is specified with the TOKN command.

3.4.2 Notation

The following table summarizes the notation used in the command descriptions:

Symbol	Definition
i	Bit number (0–7)
j	Unsigned integer (0–65535)
m	Unsigned integer (1–3)
y, z	Literal token
(?)	Required for queries; illegal for set commands
var	Parameter always required
{*var*}	Required parameter for set commands; illegal for queries
[*var*]	Optional parameter for both set and query forms

3.4.3 Examples

Each command is provided with a simple example illustrating its usage. In these examples, all data sent by the host computer to the SIM918 are set as `straight teletype font`, while responses received by the host computer from the SIM918 are set as *`slanted teletype font`*.

The usage examples vary with respect to set/query, optional parameters, and token formats. These examples are not exhaustive, and are intended to provide a convenient starting point for user programming.

3.4.4 General commands

HELP(?) Instrument Help

Outputs a condensed version of Section 3.4 to the remote interface.

HELP may be used with or without the query sign, with the same effects.

Example:

```
HELP?
Notation:
i is bit number (0..7);
j is a 16-bit unsigned integer (0..65535);
m is a small unsigned integer (1..3);
y, z are tokens
(?) question required for queries, illegal for set commands;
[] = parameter is optional for both set and query forms;
{} = parameter is required to set, illegal for queries;
parameter without brackets is always required;
the brackets themselves should not be sent.

General commands:
HELP?            - Send this text.
AWAK(?) {z}      - Keep the module clock awake.

Configuration commands:
FPLC(?) {j}      - Power line rejection frequency (50, 60).
GAIN(?) {m}      - Set/query gain.
INPT(?) {z}      - Input (OPEN, CLOSE).
BIAS(?) {z}      - Bias (GND, ON).
SHLD(?) y {,z}   - Shield (INPUT, BIAS)
                          (GND, BIAS, FLOAT, PROG).
CHOP(?) {z}      - Autozero OFF/ON.
SYNC(?) {z}      - Reference clock IN/OUT.
FREQ?            - Reference clock frequency (Hz).
PHAS?            - Switch position (Zero Amp, Zero Zero).
APLL(?) {z}      - Keep PLL active when autozero is off.

Calibration commands:
ACAL             - One-time autocalibration.
READ? m          - Check intermediate/output voltage (uV).
OFST(?) m {,j}   - Set/query offset trim.

Status commands:
*CLS             - Clear Status.
*STB?   [i]      - Query the Status Byte.
*SRE(?) [i,] {j} - Service Request Enable.
```

```
*ESR?   [i]      - Query Standard Event Status register.
*ESE(?) [i,] {j} - Standard Event Status Enable.
CESR?   [i]      - Query the Communications Error Status.
CESE(?) [i,] {j} - Communications Error Status Enable.
OLSR?   [i]      - Query Overload Status register.
OLSE(?) [i,] {j} - Overload Status Enable.
RCSR?   [i]      - Query Reference Clock Status register.
RCSE(?) [i,] {j} - Reference Clock Status Enable.
PSTA(?) {z}      - Pulse Status or change its level.
LBTN?            - Which button last pressed?
OVLD?            - Bias, intermediate, or output overloaded?
RCLK?            - Reference clock int./ext., locked?

Interface commands:
*RST             - Reset to known state.
*IDN?            - Identify.
*TST?            - Does nothing.
*OPC(?)          - Operation complete.
CONS(?) {z}      - Console OFF/ON.
LEXE?            - Last Execution Error.
LCME?            - Last Communications Error.
LDDE?            - Last Device Error.
TOKN(?) {z}      - Turn token mode OFF/ON.
TERM(?) {z}      - Cmd line end (NONE, CR, LF, CRLF, LFCR).

Serial interface command (baud rate is always 9600):
PARI(?) {z}      - Parity (NONE, EVEN, ODD, MARK, SPACE).
```

AWAK(?) {*z*} Keep Clock Awake

Set (query) the SIM918 keep-awake mode {to *z* = (**OFF 0**, ON 1)}.

Ordinarily, the clock oscillator for the SIM918 microcontroller is held in a stopped state, and only enabled during processing of events (Section 2.7). Setting AWAK ON forces the clock to stay running, and is useful only for diagnostic purposes.

Example: `AWAK ON`

3.4.5 Configuration commands

FPLC(?) {*j*}

Power Line Cycle Frequency

Set (query) the power-line rejection frequency {to *j* = (`50`, `60`)}, in Hz.

The FPLC value is retained in non-volatile memory, and is *not* modified by a power-on reset.

Example:
```
FPLC 60
```

GAIN(?) {*m*}

Gain

Set (query) the preamplifier gain {to *m*}.

Value	Gain, V/A
0	2.0×10^4
1	1.000×10^6
2	1.000×10^7
3	1.00×10^8

A special case *m* = **0** connects the input terminal to the output of the transimpedance stage through $R_F = 20\,k\Omega$. This state is indicated by all *GAIN* LEDs switched off. With *BIAS GND*, the configuration reproduces the input offset voltage at the output of the instrument. This voltage may be measured with READ? 3.

The configuration *m* = **0** is volatile, and is reset to *m* = **1** upon power-on.

Example:
```
GAIN?
2
```

INPT(?) {*z*}

Input

Set (query) the preamplifier input connection {to *z* = (`OPEN` **0**, **`CLOSE`** **1**)}.

Example:
```
INPT CLOSE
```

BIAS(?) {*z*}

Bias

Set (query) the preamplifier bias connection {to *z* = (**`GND`** **0**, `ON` 1)}.

Example:
```
BIAS?
ON
```

SHLD(?) *y* {, *z*}

Shield

Set (query) the preamplifier BNC shield connection for *y* = (`INPUT 0`, `BIAS 1`) {to *z* = (`GND 0`, `BIAS 1`, `FLOAT 2`, `PROG 3`)}.

The following combinations are valid:

BNC *y*	Shield *z*
INPUT	**GND**
	BIAS
	PROG
BIAS	**GND**
	FLOAT

Example:
```
SHLD INPUT,BIAS
SHLD BIAS,FLOAT
```

CHOP(?) {*z*}

Autozero

Set (query) the preamplifier autozero selection {to *z* = (`OFF 0`, **`ON 1`**)}. There will be a wait before the chosen regime takes effect (Section 1.2.2.1).

Example:
```
CHOP?
ON
```

SYNC(?) {*z*}

Reference Clock Direction

Set (query) the direction of the signal at the SIM918 rear-panel Ref Clock Sync connector {to *z* = (**`IN 0`**, `OUT 1`)}. The direction is reset to **`IN`** upon power-on.

Example:
```
SYNC 1
```

FREQ?

Reference Clock Frequency

Query the reference clock frequency of the preamplifier, in hertz. The nominal frequency of the internal reference clock is 1.0 Hz. The command can also be used to measure the frequency of an external reference clock.

If autozero is off and the reference clock is internal, or if autozero is off and APLL is set to `OFF` under external reference clock, there are no reference clock transitions inside the SIM918 and FREQ? will time out with Execution Error 16.

Example:
```
FREQ?
1.023
```

PHAS? Autozero Phase

Query the autozero switch position in the preamplifier. The responses are `ZA 0` (while zeroing the input voltage of the main amplifier itself) and `ZZ 1` (while zeroing the offset volage of the zeroing amplifier). These responses alternate with every cycle of the reference clock.

The switches are parked in the `ZA` state when autozero is off.

Example:
```
TOKN ON; PHAS?
ZZ
```

APLL(?) {*z*} Keep PLL Active

Set (query) the "keep PLL active when autozero is off" mode of the preamplifier {to *z* = (**`OFF 0,`** `ON 1`)}.

This setting only applies to the external reference clock direction. When APLL is `OFF`, turning off the autozero function (CHOP `OFF`) will fully halt the PLL oscillator (Section 2.5), ensuring that *no* digital clock transitions occur. One consequence of APLL `OFF` is that the oscillator will require up to 250 s to reestablish the lock to an external reference when returning to CHOP `ON`.

Conversely, with APLL `ON` the internal oscillator will continue to track an external 1 pps reference clock during CHOP `OFF` periods. In this case, there is no re-lock time needed when returning to CHOP `ON`.

The PLL oscillator always turns off with CHOP `OFF` in the internal reference clock mode.

The APLL setting is retained in non-volatile memory, and is *not* modified by a power-on reset.

Example:
```
APLL 1
```

3.4.6 Calibration commands

ACAL Autocalibration

Perform a self-calibration (Section 2.6). *Make sure to disconnect all inputs and outputs to the SIM918.* Remote commands are not processed until ACAL is complete.

Example:
```
ACAL
LDDE?
0
```
checks for success of an autocalibration.

READ? *m* — Read Microvoltmeter

Query instrument voltage *m*, in microvolts. READ? 1 queries the voltage at the overall Output terminal, and READ? 3, the voltage at the output of the transimpedance stage. These diagnostics are useful in manually adjusting the output and input offsets with the commands OFST 1 and OFST 2/OFST 3, respectively.

The command READ? 2 measures the control output of an internal digital-to-analog converter. This output adds together with the output of the autozero control loop to form the overall control output of the autozero circuit, and is adjusted with OFST 2.

Disconnect all inputs and outputs to the SIM918 before issuing READ?. Connect the center and shield terminals of the Bias BNC together externally, e.g. with a grounding cap. There will be a wait of several seconds for the command to execute while internal switches are configured and the voltages are sampled and averaged. Autozero is *ON* while READ? executes, and the reference clock is used during the measurement. The results of READ? will be unpredictable if the reference clock is external and *Unlocked*. Remote commands are not processed until READ? is complete.

Example:
```
READ? 1
-12
```

OFST(?) *m* {, *j*} — Offset Trim

Set (query) offset trim *m* {to *j*}. The trims are established by autocalibration. If needed, the offsets in the SIM918 (Section 2.4) may be adjusted manually as follows:

Trim *m*	Range of *j*	Adjusts offset	When	By
1	-128–+126	Output	BIAS ON	3.9 μV/count
2	-32768–+32767	Input	CHOP OFF	0.45 μV/count
3	-128–+126	Input	CHOP ON	0.45 μV/count

A greater value of OFST 1 will make the output voltage more positive. A greater value of OFST 2 or OFST 3 will make the input offset more positive, i.e. will make the input voltage exceed the bias voltage by more microvolts.

Example:
```
OFST? 3
-13
READ? 3
14
OFST 3,-42
```

3.4.7 Status commands

The Status commands query and configure registers associated with status reporting of the SIM918. See Section 3.5 for the status model.

---

*CLS

Clear Status

*CLS immediately clears the ESR, CESR, RCSR, and OLSR status registers.

Example:
```
*CLS
```

---

*STB? [*i*]

Status Byte

Query the Status Byte register [Bit *i*].

Execution of the *STB? query (without the optional Bit *i*) always causes the ¬STATUS signal to be deasserted. Note that *STB? *i* will *not* clear ¬STATUS, even if Bit *i* is the only bit presently causing the ¬STATUS signal.

Example:
```
*STB?
16
```

---

*SRE(?) [*i*,] {*j*}

Service Request Enable

Set (query) the Service Request Enable register [Bit *i*] {to *j*}.

Example:
```
*SRE 0,1
```

---

*ESR? [*i*]

Standard Event Status

Query the Standard Event Status Register [Bit *i*].

Upon execution of *ESR? , the returned bit(s) of the ESR register are cleared.

Example:
```
*ESR?
64
```

---

*ESE(?) [*i*,] {*j*}

Standard Event Status Enable

Set (query) the Standard Event Status Enable register [Bit *i*] {to *j*}.

Example:
```
*ESE 6,1
ESE?
64
```

CESR? [*i*] Communication Error Status

Query the Communication Error Status Register [Bit *i*].

Upon executing a CESR? query, the returned bit(s) of the CESR register are cleared.

Example:
```
CESR?
0
```

CESE(?) [*i*,] {*j*} Communication Error Status Enable

Set (query) the Communication Error Status Enable register [Bit *i*] {to *j*}.

Example:
```
CESE?
2
```

OLSR? [*i*] Overload Status

Query the Overload Status Register [Bit *i*].

Upon executing an OLSR? query, the returned bit(s) of the OLSR register are cleared.

Example:
```
OLSR?
3
```

OLSE(?) [*i*,] {*j*} Overload Status Enable

Set (query) the Overload Status Enable register [Bit *i*] {to *j*}.

Example:
```
OLSE 4
```

RCSR? [*i*] Reference Clock Status

Query the Reference Clock Status Register [Bit *i*].

Upon executing an RCSR? query, the returned bit(s) of the RCSR register are cleared.

Example:
```
RCSR?
7
```

RCSE(?) [*i*,] {*j*} Reference Clock Status Enable

Set (query) the Reference Clock Status Enable register [Bit *i*] {to *j*}.

Example:
```
RCSE 3,1
```

PSTA(?) {*z*}

Pulse ¬STATUS Mode

Set (query) the Pulse ¬STATUS mode {to *z* = (**OFF 0**, ON 1)}.

When PSTA ON is set, all new service requests will only *pulse* the ¬STATUS signal LOW (for a minimum of 1 μs). The default behavior is to latch ¬STATUS LOW until a *STB? query is received.

A reset does not alter PSTA. The value in boldface above is the power-on value.

Example:
```
PSTA OFF
```

LBTN?

Last Button

Query the number of the last button pressed. The response is

LBTN?	Last button
1	[GAIN ◄]
2	[GAIN ►]
3	[AUTOZERO]
4	[Output 1 pps sync]
5	[INPUT Open]
6	[INPUT Shield]
7	[BIAS GND]
8	[BIAS Shield]
9	Both [GAIN ◄] and [GAIN ►] (autocalibrate)
10	A button held upon power-on (reset)

The value 0 is returned if no button was pressed since the last LBTN? .

A query of LBTN? always clears the button code, so a subsequent LBTN? will return 0.

Example:
```
LBTN?
5
```

OVLD?

Overload

Query the current overload condition. The response is

OVLD?	Overloaded
1	Bias
2	Output
4	Bias + Output

Combination overloads are reported by summing the values of the individual overload flags. This command complements the OLSR status register described in Section 3.5.7, and the three overload flags correspond one-to-one with bits in OLSR. However, once cleared

by OLSR? or *CLS, the overload status bits will stay cleared even though the overload condition may persist and remain reported by OVLD? .

Example: `OVLD?`
`6`
implies that the bias is *not* overloaded; the transimpedance stage ($V_{\text{bias}} - i_{\text{in}} \times R_{\text{F}}$) *is* overloaded; and the output *is* overloaded.

RCLK? Reference Clock State

Query the current source and lock state of the reference clock of the preamplifier. The responses are `INTERNAL 0`, `EXTERNAL 1`, and `UNLOCKED 3`.

This command complements the RCSR status register described in Section 3.5.9, but there is no one-to-one correspondence between the response of RCLK? and bits in RCSR. Once cleared by RCSR? or *CLS, the reference clock status bits will stay cleared even though the reference clock state may persist and remain reported by RCLK? .

Example: `RCLK?`
`UNLOCKED`

3.4.8 Interface commands

The Interface commands provide control over the interface between the SIM918 and the host computer.

---

*RST Reset

Reset the SIM918 to its default configuration.

*RST sets the following:

1. Gain to 10^6 V/A.
2. Autozero on.
3. Input connected.
4. Input shield to ground.
5. Bias to ground.
6. Bias shield to ground.
7. Reference clock direction to input.
8. The phase-locked loop to inactive when autozero is off (APLL `OFF`).
9. Clock oscillator to stop during idle time (AWAK `OFF`).

10. The token mode to OFF.

*RST does *not* affect PSTA, CONS, TERM, and all service-enable registers (*SRE, *ESE, CESE, RCSE, or OLSE).

Example:
```
*RST
CONS?
1
```

***IDN?** — Identify

Query the device identification string.

The identification string is formatted as:

`Stanford_Research_Systems,SIM918,s/n******,ver#.###`

where SIM918 is the model number, ****** is a 6-digit serial number, and #.### is the firmware revision level.

Example:
```
*IDN?
Stanford_Research_Systems,SIM918,s/n005432,ver2.1
```

***TST?** — Self Test

There is no internal self-test in the SIM918 after the power-on, so this query always returns **0**.

Example:
```
*TST?
0
```

***OPC(?)** — Operation Complete

Sets the OPC flag in the ESR register.

The query form *OPC? writes a 1 into the output queue when complete, but does not affect the ESR register.

Example:
```
*OPC?
1
```

CONS(?) {*z*} — Console Mode

Set (query) the console mode {to *z* = (**OFF 0**, ON 1)}.

CONS causes each character received at the input buffer to be copied to the output queue.

A reset does not alter CONS. The value in boldface above is the power-on value. CONS is set to OFF upon Device Clear.

Example:
```
CONS ON
```

LEXE? Execution Error

Query the Last Execution Error code. A query of LEXE? always clears the error code, so a subsequent LEXE? will return 0. Valid codes are:

Value	Definition
0	No execution error since last LEXE?
1	Illegal value
2	Wrong token
3	Invalid bit
16	Reference clock inactive

Example:
```
*STB? 12; LEXE?; LEXE?
3
0
```
The error (3, "Invalid bit") is because *STB? only allows bit-specific queries of 0–7. The second read of LEXE? returns 0.

LCME? Command Error

Query the Last Command Error code. A query of LCME? always clears the error code, so a subsequent LCME? will return 0. Valid codes are:

Value	Definition
0	No command error since last LCME?
1	Illegal command
2	Undefined command
3	Illegal query
4	Illegal set
5	Missing parameter(s)
6	Extra parameter(s)
7	Null parameter(s)
8	Parameter buffer overflow
10	Bad integer
11	Bad integer token
12	Bad token value
14	Unknown token

Example:
```
*IDN
LCME?
4
```
The error (4, "Illegal set") is due to the missing "?".

LDDE? Device Error

Query the Last Device-Dependent Error code. A query of LDDE? always clears the error code, so a subsequent LDDE? will return `0`. Valid codes are:

Value	Definition
0	No execution error since last LEXE?
1	Reference clock conflict
2	Unable to autocalibrate

Example:
```
ACAL
LDDE?
0
```
indicates a successful autocalibration.

TOKN(?) {*z*} Token Mode

Set (query) the token query mode {to *z* = (**`OFF 0`**, `ON 1`)}.

If TOKN `ON` is set, then queries to the SIM918 that return tokens will return a text keyword; otherwise they return a decimal integer value. Thus, the only possible responses to the TOKN? query are `ON` and `0`.

Example:
```
TOKN OFF
```

TERM(?) {*z*} Response Termination

Set (query) the ⟨term⟩ sequence {to *z* = (`NONE 0`, `CR 1`, `LF 2`, **`CRLF 3`**, or `LFCR 4`)}.

The ⟨term⟩ sequence is appended to all query responses sent by the module, and is constructed of ASCII character(s) 13 (carriage return) and 10 (line feed). The token mnemonic gives the sequence of characters.

A reset does not alter TERM. The value in boldface above is the power-on value.

Example:
```
TOKN ON; TERM?
CRLF
```

3.4.9 Serial communication commands

Note that the SIM918 can only support a single baud rate of 9600, and does not support flow control. A reset does not change the serial interface settings; use Device Clear.

PARI(?) {*z*} Parity

Set (query) the parity {to *z* = (**NONE 0,** ODD 1, EVEN 2, MARK 3, SPACE 4)}. The value in boldface is the power-on value.

Example:
```
TOKN ON; PARI?
EVEN
```

3.5 Status Model

status registers The SIM918 status registers follow the hierarchical IEEE–488.2 format. A block diagram of the status register array is given in Figure 3.1.

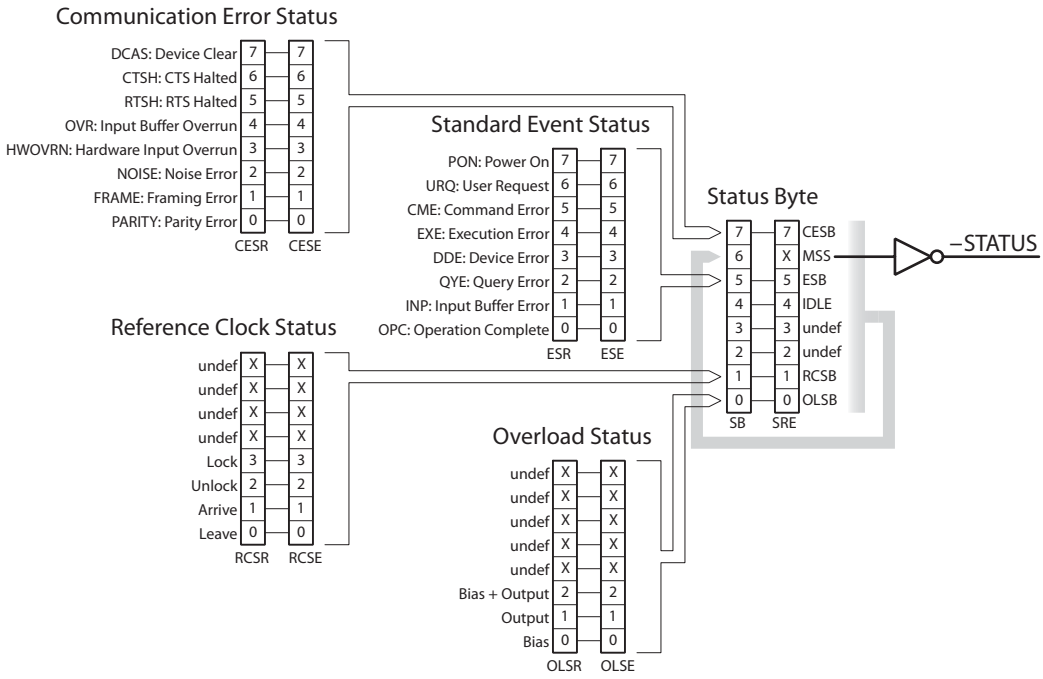


Figure 3.1: Status register model for the SIM918 Precision Current Preamplifier.

There are two categories of registers in the SIM918 status model:

Event Registers : These read-only registers record the occurrence of defined events. If the event occurs, the corresponding bit is set to 1. Upon querying an event register, all set bits within it are cleared. These are sometimes known as "sticky bits," since once set, a bit can only be cleared by reading its value. Event register names end with SR.

Enable Registers : These read/write registers define a bitwise mask for their corresponding event register. If a bit position is set in an event register while the same bit position is also set in the enable register, then the corresponding summary bit message is set. Enable register names end with SE.

At power-on, all status registers are cleared.

3.5.1 Status Byte (SB)

The Status Byte is the top-level summary of the SIM918 status model. When masked by the Service Request Enable register, a bit set in the Status Byte causes the ¬STATUS signal to be asserted on the rear-panel SIM interface connector.

Weight	Bit	Flag
1	0	OLSB
2	1	RCSB
4	2	undef (0)
8	3	undef (0)
16	4	IDLE
32	5	ESB
64	6	MSS
128	7	CESB

OLSB : Overload Summary Bit. Indicates whether one or more of the enabled flags in the Overload Status Register has become true.

RCSB : Reference Clock Summary Bit. Indicates whether one or more of the enabled flags in the Reference Clock Status Register has become true.

IDLE : Indicates that the input buffer is empty and the command parser is idle. Can be used to help synchronize SIM918 query responses.

ESB : Event Status Bit. Indicates whether one or more of the enabled events in the Standard Event Status Register is true.

MSS : Master Summary Status. Indicates whether one or more of the enabled status messages in the Status Byte register is true.

CESB : Communication Error Summary Bit. Indicates whether one or more of the enabled flags in the Communication Error Status Register has become true.

3.5.2 Service Request Enable (SRE)

Each bit in the SRE corresponds one-to-one with a bit in the SB register, and acts as a bitwise AND of the SB flags to generate MSS. Bit 6 of the SRE is undefined—setting it has no effect, and reading it always returns 0. This register is set and queried with the *SRE(?) command.

At power-on, this register is cleared.

3.5.3 Standard Event Status (ESR)

The Standard Event Status Register consists of 8 event flags. These event flags are all "sticky bits" that are set by the corresponding events, and cleared only by reading or with the *CLS command. Reading a single bit (with the *ESR? *i* query) clears only Bit *i*.

Weight	Bit	Flag
1	0	OPC
2	1	INP
4	2	QYE
8	3	DDE
16	4	EXE
32	5	CME
64	6	URQ
128	7	PON

OPC : Operation Complete. Set by the *OPC command.

INP : Input buffer error. Indicates data has been discarded from the input buffer.

QYE : Query Error. Indicates data in the output queue has been lost.

DDE : Device-Dependent Error. Indicates a failed autocalibration or a reference clock conflict.

EXE : Execution Error. Indicates the error in a command that was successfully parsed. Out-of-range parameters are an example.

CME : Command Error. Indicates a command parser-detected error.

URQ : User Request. Indicates that a front-panel button was pressed.

PON : Power On. Indicates that an off-to-on transition has occurred.

3.5.4 Standard Event Status Enable (ESE)

The ESE acts as a bitwise AND with the ESR register to produce the single-bit ESB message in the Status Byte Register (SB). The register can be set and queried with the *ESE(?) command.

At power-on, this register is cleared.

3.5.5 Communication Error Status (CESR)

The Communication Error Status Register consists of 8 event flags; each of the flags is set by the corresponding event, and cleared only by reading the register or with the *CLS command. Reading a single bit (with the CESR? *i* query) clears only Bit *i*.

Weight	Bit	Flag
1	0	PARITY
2	1	FRAME
4	2	NOISE
8	3	HWOVRN
16	4	OVR
32	5	RTSH
64	6	CTSH
128	7	DCAS

PARITY : Parity error. Set by serial parity mismatch on the incoming data byte.

FRAME : Framing error. Set when an incoming serial data byte is missing the STOP bit.

NOISE : Noise error. Set when an incoming serial data byte does not present a steady logic level during each asynchronous bit-period window.

HWOVRN : Hardware Overrun. Set when an incoming serial data byte is lost due to internal processor latency. Causes the input buffer to be flushed, and resets the command parser.

OVR : Input buffer Overrun. Set when the input buffer is overrun by the incoming data. Causes the input buffer to be flushed, and resets the command parser.

RTSH : RTS Holdoff Event. Unused in the SIM918.

CTSH : CTS Holdoff Event. Unused in the SIM918.

DCAS : Device Clear. Indicates that the SIM918 received the Device Clear signal (an RS–232 ⟨break⟩). Clears the input buffer and the output queue, and resets the command parser.

3.5.6 Communication Error Status Enable (CESE)

The CESE acts as a bitwise AND with the CESR register to produce the single-bit CESB message in the Status Byte Register (SB). The register can be set and queried with the CESE(?) command.

At power-on, this register is cleared.

3.5.7 Overload Status (OLSR)

The Overload Status Register consists of 3 event flags; each of the flags is set by the corresponding overload, and cleared only by reading the register or with the *CLS command. Reading a single bit (with the OLSR? *i* query) clears only Bit *i*.

Weight	Bit	Flag
1	0	Bias
2	1	Output
4	2	Bias + Output
8	3	undef (0)
16	4	undef (0)
32	5	undef (0)
64	6	undef (0)
128	7	undef (0)

Bias : Bias overload. Indicates that $|V_{\text{bias}}| > 5.0\,\text{V}$ (see also Section 1.2.4.1).

Output : Output overload. Indicates that $|V_{\text{out}}| > 10.0\,\text{V}$ (see also Section 1.2.5).

Bias + Output : Transimpedance stage overload. Indicates that $|V_{\text{bias}} - i_{\text{in}} \times R_{\text{F}}| > 10.0\,\text{V}$.

Reading this register (with the OLSR? query) clears all overload bits that are set. If the overload condition persists, the bits will remain cleared until the overload condition ceases and reoccurs. Use OVLD? to query the current state of the overload.

3.5.8 Overload Status Enable (OLSE)

The OLSE acts as a bitwise AND with the OLSR register to produce the single-bit OLSB message in the Status Byte Register (SB). The register can be set and queried with the OLSE(?) command.

At power-on, this register is cleared.

3.5.9 Reference Clock Status (RCSR)

The Reference Clock Status Register consists of 4 event flags; each of the flags is set by the corresponding clock event, and cleared only by reading the register or with the *CLS command. Reading a single bit (with the RCSR? *i* query) clears only Bit *i*.

Weight	Bit	Flag
1	0	Leave
2	1	Arrive
4	2	Unlock
8	3	Lock
16	4	undef (0)
32	5	undef (0)
64	6	undef (0)
128	7	undef (0)

Leave : Reference clock stop detect. Indicates that the external reference clock signal has ceased.

Arrive : Reference clock start detect. Indicates that several periodic clock edges have been newly present at the rear-panel Ref Clock Sync connector.

Unlock : Unlock detect. Indicates that the reference clock PLL (Section 2.5) has transitioned from locked or idle to unlocked.

Lock : Lock detect. Indicates that the reference clock PLL has transitioned from unlocked to locked.

Reading this register (with the RCSR? query) clears all event bits that are set. If the clock state persists (e.g. the clock remains unlocked), the bits will remain cleared until the state ceases and reoccurs. Use RCLK? to query the current state of the reference clock.

3.5.10 Reference Clock Status Enable (RCSE)

The RCSE acts as a bitwise AND with the RCSR register to produce the single-bit RCSB message in the Status Byte Register (SB). The register can be set and queried with the RCSE(?) command.

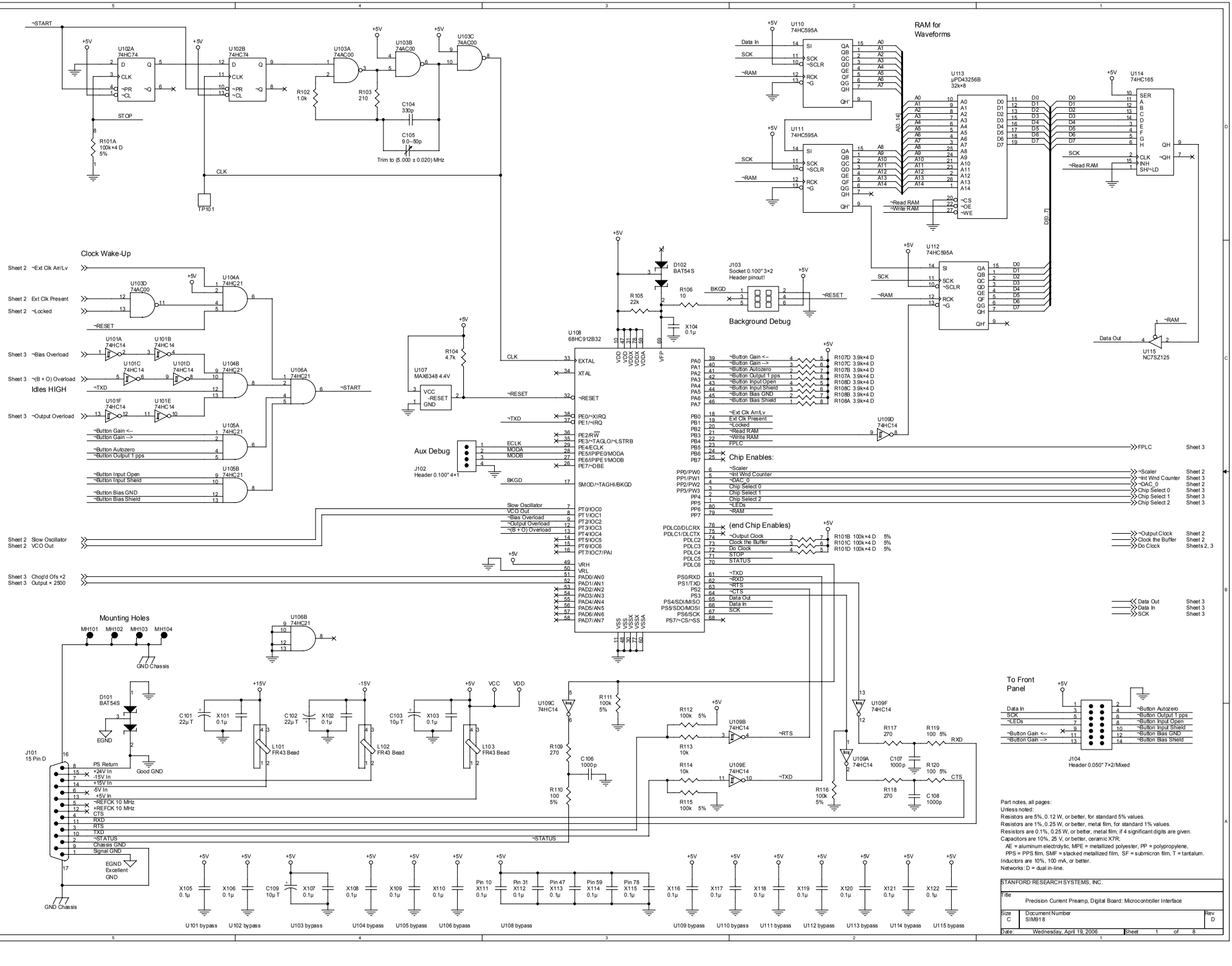
At power-on, this register is cleared.

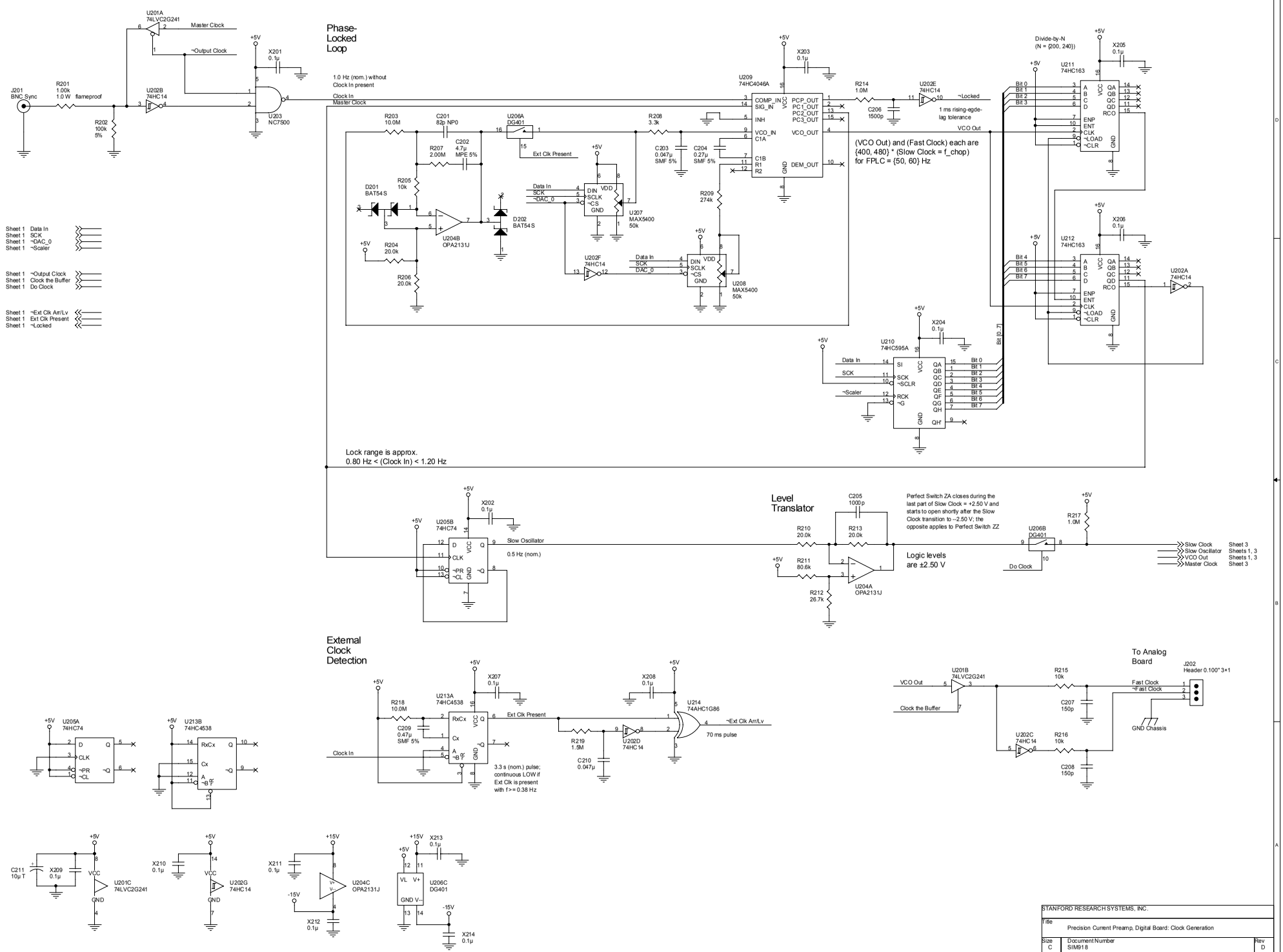
4 Circuit Description

In This Chapter

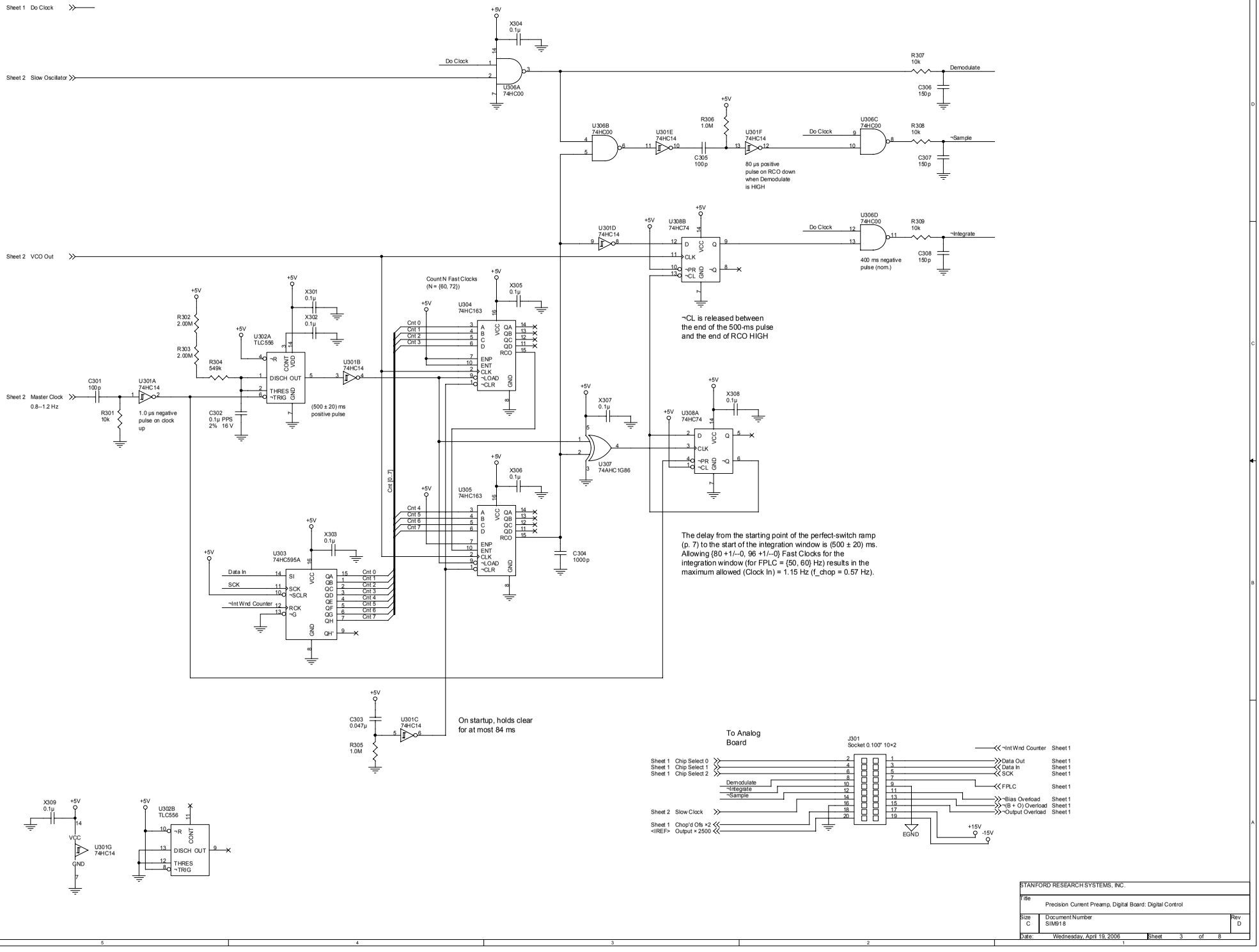
4.1 Schematic Diagrams

Circuit schematic diagrams follow this page.


¬START
U102A 74HC74
U102B 74HC74
U103A 74AC00
U103B 74AC00
U103C 74AC00
R102 1.0k
R103 210
C104 330p
C105 9.0–50p
Trim to (5.000 ± 0.020) MHz
STOP
R101A 100k×4 D 5%
TP101
CLK
RAM for Waveforms
U110 74HC595A
U111 74HC595A
U112 74HC595A
U113 μPD43256B 32k×8
U114 74HC165
U115 NC7SZ125
Data In
SCK
¬SCLR
¬RAM
¬G
RCK
QA QB QC QD QE QF QG QH QH'
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
D0 D1 D2 D3 D4 D5 D6 D7
¬CS ¬OE ¬WE
¬Read RAM
¬Write RAM
SER A B C D E F G H
CLK INH SH/¬LD
Clock Wake-Up
Sheet 2 ¬Ext Clk Arr/Lv
Sheet 2 Ext Clk Present
Sheet 2 ¬Locked
¬RESET
Sheet 3 ¬Bias Overload
Sheet 3 ¬(B + O) Overload
¬TXD
Idles HIGH
Sheet 3 ¬Output Overload
¬Button Gain <--
¬Button Gain -->
¬Button Autozero
¬Button Output 1 pps
¬Button Input Open
¬Button Input Shield
¬Button Bias GND
¬Button Bias Shield
¬START
U101A 74HC14
U101B 74HC14
U101C 74HC14
U101D 74HC14
U101E 74HC14
U101F 74HC14
U103D 74AC00
U104A 74HC21
U104B 74HC21
U105A 74HC21
U105B 74HC21
U106A 74HC21
U107 MAX6348 4.4V
VCC ¬RESET GND
R104 4.7k
D102 BAT54S
R105 22k
R106 10
X104 0.1μ
J103 Socket 0.100" 3×2 Header pinout!
BKGD
Background Debug
Aux Debug
J102 Header 0.100" 4×1
ECLK
MODA
MODB
U108 68HC912B32
VDD VDDX VDDA VFP
VSS VSSX VSSA
EXTAL
XTAL
¬RESET
PE0/¬XIRQ
PE1/¬IRQ
PE2/R/¬W
PE3/¬TAGLO/¬LSTRB
PE4/ECLK
PE5/IPIPE0/MODA
PE6/IPIPE1/MODB
PE7/¬DBE
SMOD/¬TAGHI/BKGD
Slow Oscillator
VCO Out
¬Bias Overload
¬Output Overload
¬(B + O) Overload
VRH
VRL
PAD0/AN0
PAD1/AN1
PAD2/AN2
PAD3/AN3
PAD4/AN4
PAD5/AN5
PAD6/AN6
PAD7/AN7
PT0/IOC0
PT1/IOC1
PT2/IOC2
PT3/IOC3
PT4/IOC4
PT5/IOC5
PT6/IOC6
PT7/IOC7/PAI
PA0 ¬Button Gain <--
PA1 ¬Button Gain -->
PA2 ¬Button Autozero
PA3 ¬Button Output 1 pps
PA4 ¬Button Input Open
PA5 ¬Button Input Shield
PA6 ¬Button Bias GND
PA7 ¬Button Bias Shield
R107D 3.9k×4 D
R107C 3.9k×4 D
R107B 3.9k×4 D
R107A 3.9k×4 D
R108D 3.9k×4 D
R108C 3.9k×4 D
R108B 3.9k×4 D
R108A 3.9k×4 D
PB0 ¬Ext Clk Arr/Lv
PB1 Ext Clk Present
PB2 ¬Locked
PB3 ¬Read RAM
PB4 ¬Write RAM
PB5 FPLC
PB6
PB7
Chip Enables:
PP0/PW0 ¬Scaler
PP1/PW1 ¬Int Wnd Counter
PP2/PW2 ¬DAC_0
PP3/PW3 Chip Select 0
PP4 Chip Select 1
PP5 Chip Select 2
PP6 ¬LEDs
PP7 ¬RAM
PDLC0/DLCRX
PDLC1/DLCTX
(end Chip Enables)
PDLC2 ¬Output Clock
PDLC3 Clock the Buffer
PDLC4 Do Clock
PDLC5 STOP
PDLC6 STATUS
PS0/RXD ¬TXD
PS1/TXD ¬RXD
PS2 ¬RTS
PS3 ¬CTS
PS4/SDI/MISO Data Out
PS5/SDO/MOSI Data In
PS6/SCK SCK
PS7/¬CS/¬SS
R101B 100k×4 D 5%
R101C 100k×4 D 5%
R101D 100k×4 D 5%
U109D 74HC14
FPLC Sheet 3
¬Scaler Sheet 2
¬Int Wnd Counter Sheet 3
¬DAC_0 Sheet 2
Chip Select 0 Sheet 3
Chip Select 1 Sheet 3
Chip Select 2 Sheet 3
¬Output Clock Sheet 2
Clock the Buffer Sheet 2
Do Clock Sheets 2, 3
Data Out Sheet 3
Data In Sheet 3
SCK Sheet 3
Sheet 2 Slow Oscillator
Sheet 2 VCO Out
Sheet 3 Chop'd Ofs ×2
Sheet 3 Output × 2500
Mounting Holes
MH101 MH102 MH103 MH104
GND Chassis
U106B 74HC21
D101 BAT54S
EGND
Good GND
J101 15 Pin D
PS Return
+24V In
-15V In
+15V In
-5V In
+5V In
¬REFCK 10 MHz
+REFCK 10 MHz
CTS
RXD
RTS
TXD
¬STATUS
Chassis GND
Signal GND
EGND Excellent GND
GND Chassis
C101 22μ T
X101 0.1μ
L101 FR43 Bead
C102 22μ T
X102 0.1μ
L102 FR43 Bead
C103 10μ T
X103 0.1μ
L103 FR43 Bead
U109C 74HC14
R111 100k 5%
R109 270
C106 1000p
R110 100 5%
R112 100k 5%
U109B 74HC14
R113 10k
R114 10k
U109E 74HC14
R115 100k 5%
U109F 74HC14
U109A 74HC14
R116 100k 5%
R117 270
R119 100 5%
C107 1000p
R120 100 5%
R118 270
C108 1000p
To Front Panel
J104 Header 0.050" 7×2/Mixed
X105 0.1μ
X106 0.1μ
C109 10μ T
X107 0.1μ
X108 0.1μ
X109 0.1μ
X110 0.1μ
Pin 10 X111 0.1μ
Pin 31 X112 0.1μ
Pin 47 X113 0.1μ
Pin 59 X114 0.1μ
Pin 78 X115 0.1μ
X116 0.1μ
X117 0.1μ
X118 0.1μ
X119 0.1μ
X120 0.1μ
X121 0.1μ
X122 0.1μ
U101 bypass
U102 bypass
U103 bypass
U104 bypass
U105 bypass
U106 bypass
U108 bypass
U109 bypass
U110 bypass
U111 bypass
U112 bypass
U113 bypass
U114 bypass
U115 bypass
Part notes, all pages:
Unless noted:
Resistors are 5%, 0.12 W, or better, for standard 5% values.
Resistors are 1%, 0.25 W, or better, metal film, for standard 1% values.
Resistors are 0.1%, 0.25 W, or better, metal film, if 4 significant digits are given.
Capacitors are 10%, 25 V, or better, ceramic X7R;
AE = aluminum electrolytic, MPE = metallized polyester, PP = polypropylene,
PPS = PPS film, SMF = stacked metallized film, SF = submicron film, T = tantalum.
Inductors are 10%, 100 mA, or better.
Networks: D = dual in-line.
STANFORD RESEARCH SYSTEMS, INC.
Title
Precision Current Preamp, Digital Board: Microcontroller Interface
Size C
Document Number SIM918
Rev D
Date: Wednesday, April 19, 2006
Sheet 1 of 8



STANFORD RESEARCH SYSTEMS, INC.	
Title	Precision Current Preamp, Digital Board: Clock Generation
Size C	Document Number SIM918
Rev	D
Date: Wednesday, April 19, 2006	Sheet 2 of 8



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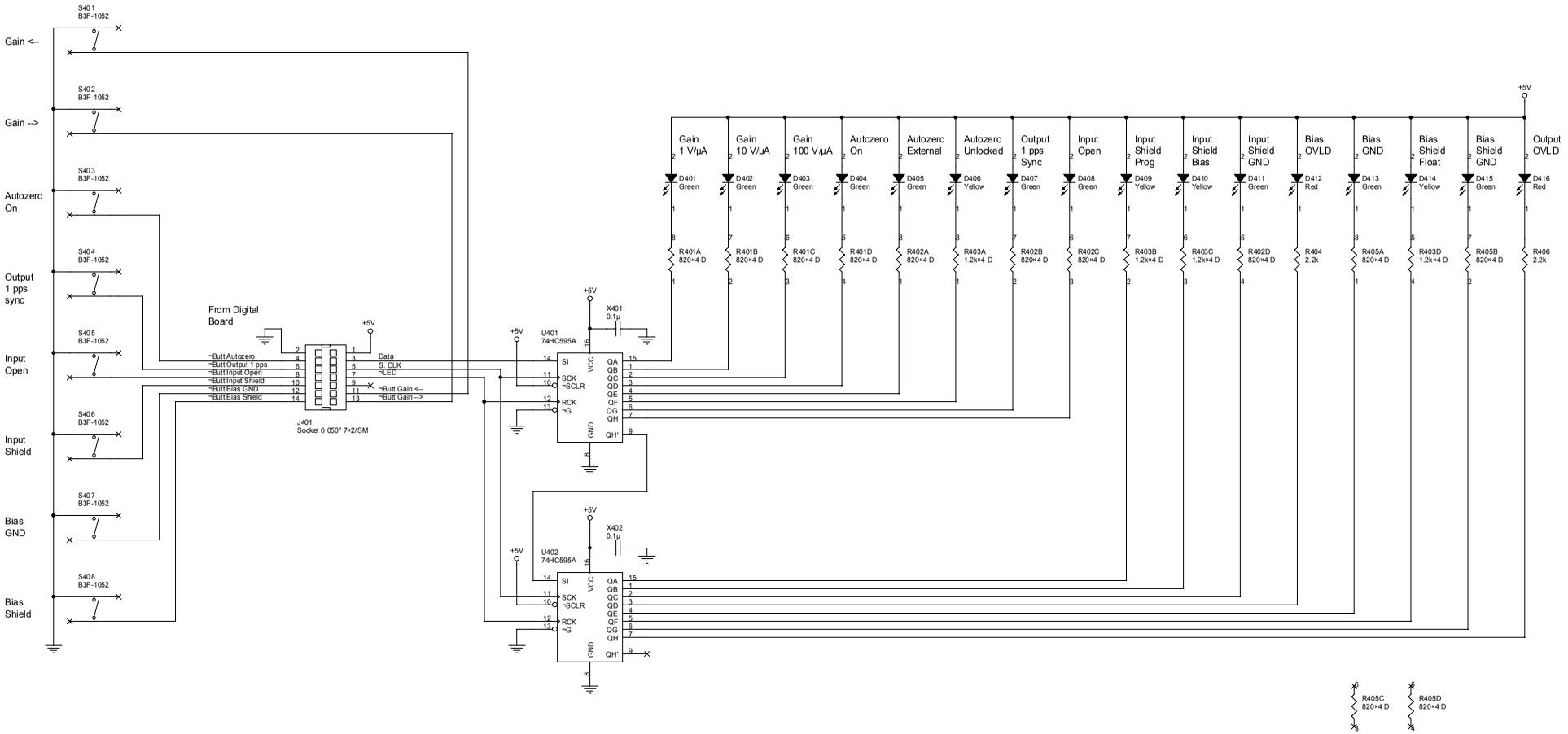
Size: C	Document Number: SIM918	Rev: D
Date: Wednesday, April 19, 2006	Sheet 3 of 8	



STANFORD RESEARCH SYSTEMS, INC.		
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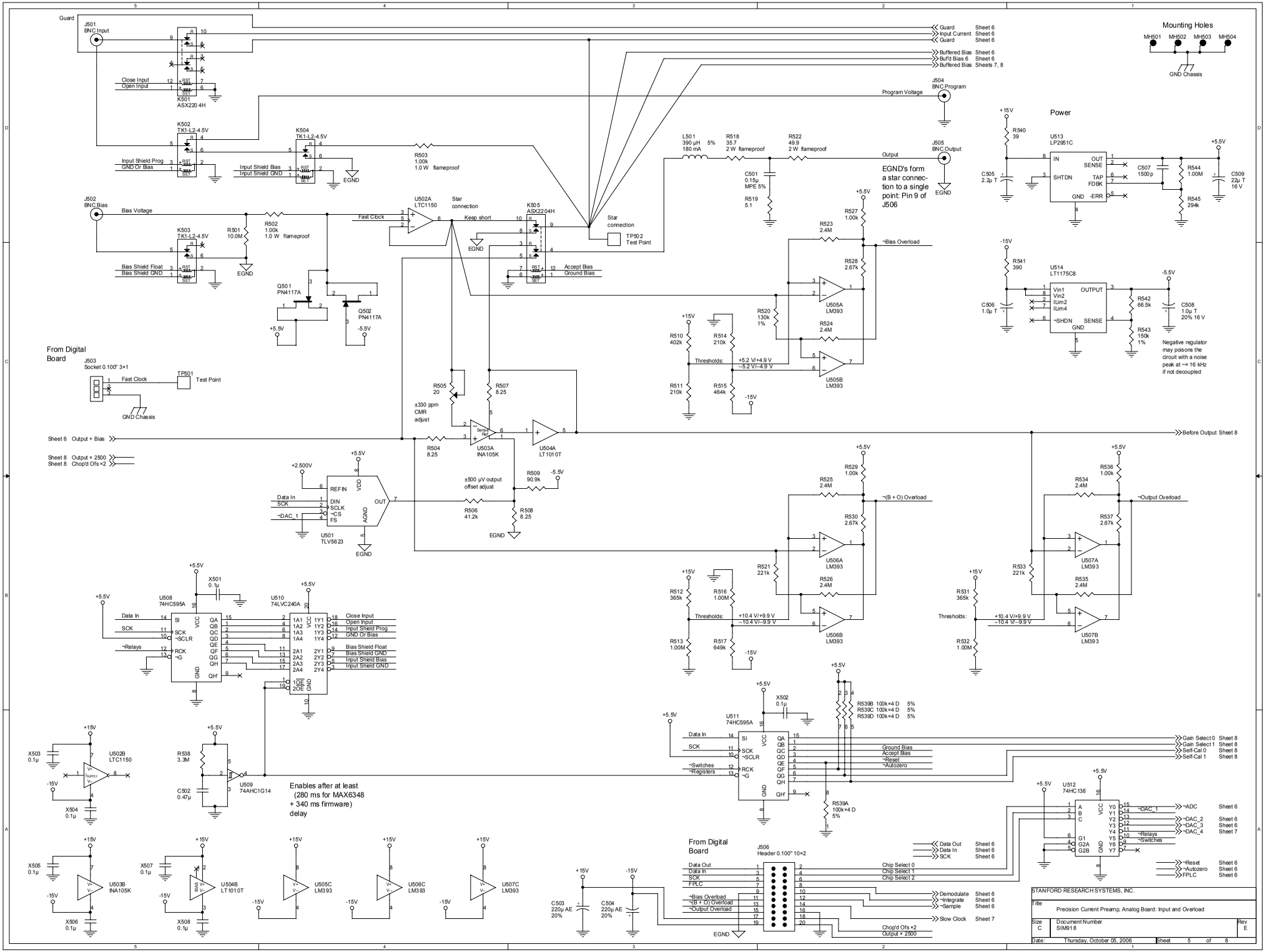
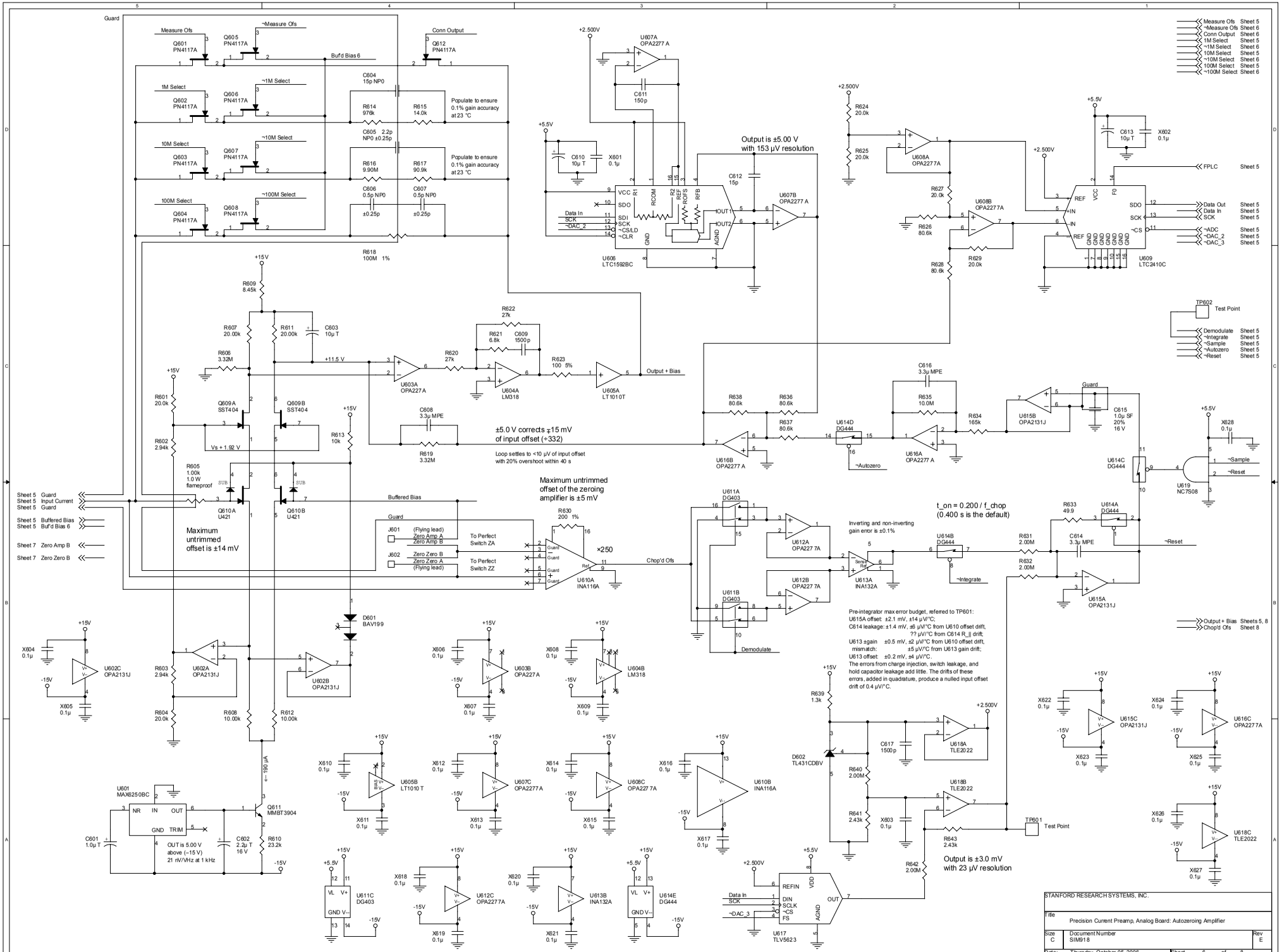
Size: C	Document Number: SIM918	Rev: D
Date: Wednesday, April 19, 2006	Sheet 4 of 8	


Guard
J501 BNC Input
Close Input
Open Input
K501 ASX220 4H
K502 TK1-L2-4.5V
Input Shield Prog
GND Or Bias
K504 TK1-L2-4.5V
Input Shield Bias
Input Shield GND
R503 1.00k 1.0 W flameproof
EGND
J502 BNC Bias
Bias Voltage
K503 TK1-L2-4.5V
Bias Shield Float
Bias Shield GND
R501 10.0M
R502 1.00k 1.0 W flameproof
Q501 PN4117A
Q502 PN4117A
+5.5V
-5.5V
Fast Clock
U502A LTC1150
Star connection
Keep short
K505 ASX2204H
Accept Bias
Ground Bias
Star connection
TP502 Test Point
Guard Sheet 6
Input Current Sheet 6
Guard Sheet 6
Buffered Bias Sheet 6
Buf'd Bias 6 Sheet 6
Buffered Bias Sheets 7, 8
Mounting Holes
MH501 MH502 MH503 MH504
GND Chassis
J504 BNC Program
Program Voltage
L501 390 µH 5% 180 mA
R518 35.7 2 W flameproof
R522 49.9 2 W flameproof
Output
J505 BNC Output
C501 0.15µ MPE 5%
R519 5.1
EGND's form a star connection to a single point: Pin 9 of J506
Power
+15V
R540 39
U513 LP2951C
IN
SHTDN
OUT
SENSE
TAP
FDBK
GND
-ERR
C505 2.2µ T
C507 1500p
R544 1.00M
R545 294k
C509 22µ T 16 V
-15V
R541 390
U514 LT1175C8
Vin1
Vin2
ILim2
ILim4
¬SHDN
OUTPUT
SENSE
GND
C506 1.0µ T
R542 66.5k
R543 150k 1%
C508 1.0µ T 20% 16 V
Negative regulator may poisons the circuit with a noise peak at ~= 16 kHz if not decoupled
R523 2.4M
R527 1.00k
¬Bias Overload
R528 2.67k
U505A LM393
R520 130k 1%
R524 2.4M
U505B LM393
R510 402k
R514 210k
Thresholds:
+5.2 V/+4.9 V
−5.2 V/−4.9 V
R511 210k
R515 464k
From Digital Board
J503 Socket 0.100" 3×1
TP501 Test Point
Fast Clock
GND Chassis
R505 20
±330 ppm CMR adjust
R507 8.25
U503A INA105K
U504A LT1010T
Sheet 6 Output + Bias
Sheet 8 Output × 2500
Sheet 8 Chop'd Ofs ×2
Before Output Sheet 8
+2.500V
U501 TLV5623
REFIN
VDD
DIN
SCLK
¬CS
FS
OUT
AGND
Data In
SCK
¬DAC_1
±500 µV output offset adjust
R509 90.9k
R506 41.2k
R508 8.25
R525 2.4M
R529 1.00k
¬(B + O) Overload
R530 2.67k
U506A LM393
R521 221k
R526 2.4M
U506B LM393
R512 365k
R516 1.00M
R513 1.00M
R517 649k
R536 1.00k
R534 2.4M
¬Output Overload
R537 2.67k
U507A LM393
R533 221k
R535 2.4M
U507B LM393
R531 365k
R532 1.00M
X501 0.1µ
U508 74HC595A
U510 74LVC240A
SI
SCK
¬SCLR
RCK
¬G
QA QB QC QD QE QF QG QH
QH'
GND
VCC
1A1 1A2 1A3 1A4
2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4
2Y1 2Y2 2Y3 2Y4
1OE 2OE
¬Relays
Close Input
Open Input
Bias Shield Float
Bias Shield GND
Input Shield Prog
GND Or Bias
Input Shield Bias
Input Shield GND
X502 0.1µ
U511 74HC595A
R539B 100k×4 D 5%
R539C 100k×4 D 5%
R539D 100k×4 D 5%
Ground Bias
Accept Bias
¬Reset
¬Autozero
¬Switches
¬Registers
R539A 100k×4 D 5%
Gain Select 0 Sheet 8
Gain Select 1 Sheet 8
Self-Cal 0 Sheet 8
Self-Cal 1 Sheet 8
X503 0.1µ
U502B LTC1150
X504 0.1µ
R538 3.3M
C502 0.47µ
U509 74AHC1G14
Enables after at least (280 ms for MAX6348 + 340 ms firmware) delay
U512 74HC138
A
B
C
G1
G2A
G2B
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
¬DAC_1
¬DAC_2
¬DAC_3
¬DAC_4
¬Relays
¬Switches
¬ADC Sheet 6
¬DAC_1 Sheet 6
¬DAC_2 Sheet 6
¬DAC_3 Sheet 6
¬DAC_4 Sheet 7
¬Reset Sheet 6
¬Autozero Sheet 6
FPLC Sheet 6
X505 0.1µ
U503B INA105K
X506 0.1µ
X507 0.1µ
U504B LT1010T
X508 0.1µ
U505C LM393
U506C LM393
U507C LM393
C503 220µ AE 20%
C504 220µ AE 20%
From Digital Board
J506 Header 0.100" 10×2
Data Out
Data In
SCK
FPLC
¬Bias Overload
¬(B + O) Overload
¬Output Overload
Chip Select 0
Chip Select 1
Chip Select 2
Demodulate Sheet 6
¬Integrate Sheet 6
¬Sample Sheet 6
Slow Clock Sheet 7
Chop'd Ofs ×2
Output × 2500
Data Out Sheet 6
Data In Sheet 6
SCK Sheet 6
STANFORD RESEARCH SYSTEMS, INC.
Title
Precision Current Preamp, Analog Board: Input and Overload
Size C
Document Number SIM918
Rev E
Date: Thursday, October 05, 2006
Sheet 5 of 8


Guard
Measure Ofs
¬Measure Ofs
Conn Output
Buf'd Bias 6
1M Select
¬1M Select
10M Select
¬10M Select
100M Select
¬100M Select
Q601 PN4117A
Q605 PN4117A
Q612 PN4117A
Q602 PN4117A
Q606 PN4117A
Q603 PN4117A
Q607 PN4117A
Q604 PN4117A
Q608 PN4117A
C604 15p NP0
C605 2.2p NP0 ±0.25p
C606 0.5p NP0 ±0.25p
C607 0.5p NP0 ±0.25p
R614 976k
R615 14.0k
R616 9.90M
R617 90.9k
R618 100M 1%
Populate to ensure 0.1% gain accuracy at 23 °C
+2.500V
U607A OPA2277 A
C611 150p
+5.5V
C610 10µ T
X601 0.1µ
U606 LTC1592BC
Data In
SCK
¬DAC_2
¬CSJLD
¬CLR
SDO
SDI
Output is ±5.00 V with 153 µV resolution
C612 15p
U607B OPA2277 A
R624 20.0k
R625 20.0k
U608A OPA2277A
R627 20.0k
U608B OPA2277A
R626 80.6k
R628 80.6k
R629 20.0k
C613 10µ T
X602 0.1µ
U609 LTC2410C
FPLC
Data Out
Data In
SCK
¬CS
¬ADC
¬DAC_2
¬DAC_3
TP602
Test Point
Demodulate
¬Integrate
¬Sample
¬Autozero
¬Reset
+15V
R609 8.45k
R607 20.00k
R611 20.00k
C603 10µ T
R606 3.32M
+11.5 V
R620 27k
R622 27k
R621 6.8k
C609 1500 p
R623 100 5%
U603A OPA227 A
U604A LM318
U605A LT1010T
Output + Bias
R601 20.0k
Q609A SST404
Q609B SST404
R602 2.94k
Vs + 1.92 V
R613 10k
C808 3.3µ MPE
R619 3.32M
±5.0 V corrects ±15 mV of input offset (÷332)
Loop settles to <10 µV of input offset with 20% overshoot within 40 s
R638 80.6k
R636 80.6k
R637 80.6k
U616B OPA2277 A
U614D DG444
¬Autozero
C616 3.3µ MPE
R635 10.0M
U616A OPA2277 A
R634 165k
U615B OPA2131J
Guard
C615 1.0µ SF 20% 16 V
U614C DG444
X828 0.1µ
U619 NC7S08
¬Sample
¬Reset
R605 1.00k 1.0 W flameproof
Q610A U421
Q610B U421
SUB
Sheet 5 Guard
Sheet 5 Input Current
Sheet 5 Guard
Sheet 5 Buffered Bias
Sheet 5 Buf'd Bias 6
Sheet 7 Zero Amp B
Sheet 7 Zero B
Maximum untrimmed offset is ±14 mV
Buffered Bias
Maximum untrimmed offset of the zeroing amplifier is ±5 mV
R630 200 1%
×250
J601 (Flying lead) Zero Amp A Zero Amp B
J602 Zero Zero B Zero Zero A (Flying lead)
To Perfect Switch ZA
To Perfect Switch ZZ
U610A INA116A
Chop'd Ofs
U611A DG403
U611B DG403
U612A OPA227 7A
U612B OPA227 7A
Demodulate
Inverting and non-inverting gain error is ±0.1%
U613A INA132A
t_on = 0.200 / f_chop
(0.400 s is the default)
U614B DG444
¬Integrate
R633 49.9
U614A DG444
¬Reset
R631 2.00M
R632 2.00M
C614 3.3µ MPE
U615A OPA2131J
Pre-integrator max error budget, referred to TP601:
U615A offset: ±2.1 mV, ±14 µV/°C;
C614 leakage: ±1.4 mV, ±6 µV/°C from U610 offset drift,
?? µV/°C from C614 R_|| drift;
U613 ±gain mismatch: ±0.5 mV, ±2 µV/°C from U610 offset drift, ±5 µV/°C from U613 gain drift;
U613 offset: ±0.2 mV, ±4 µV/°C.
The errors from charge injection, switch leakage, and hold capacitor leakage add little. The drifts of these errors, added in quadrature, produce a nulled input offset drift of 0.4 µV/°C.
Output + Bias Sheets 5, 8
Chop'd Ofs Sheet 8
R639 1.3k
D602 TL431CDBV
U618A TLE2022
C617 1500 p
R640 2.00M
R641 2.43k
U618B TLE2022
R643 2.43k
R642 2.00M
TP601 Test Point
Output is ±3.0 mV with 23 µV resolution
U617 TLV5623
REFIN
DIN
SCLK
¬CS
FS
VDD
AGND
OUT
Data In
SCK
¬DAC_3
D601 BAV199
R603 2.94k
R604 20.0k
R608 10.00k
R612 10.00k
U602A OPA2131J
U602B OPA2131J
U602C OPA2131J
X604 0.1µ
X605 0.1µ
U601 MAX6250BC
NR IN OUT GND TRIM
OUT is 5.00 V above (−15 V) 21 nV/√Hz at 1 kHz
C601 1.0µ T
C602 2.2µ T 16 V
R610 23.2k
+/− 150 µA
U611 MMBT3904
U605B LT1010 T
U603B OPA227 A
U604B LM318
U607C OPA2277 A
U608C OPA2277 A
U610B INA116A
U611C DG403
U612C OPA2277A
U613B INA132A
U614E DG444
X606 0.1µ
X607 0.1µ
X608 0.1µ
X609 0.1µ
X610 0.1µ
X611 0.1µ
X612 0.1µ
X613 0.1µ
X614 0.1µ
X615 0.1µ
X616 0.1µ
X617 0.1µ
X618 0.1µ
X619 0.1µ
X620 0.1µ
X621 0.1µ
X622 0.1µ
X623 0.1µ
X624 0.1µ
X625 0.1µ
X626 0.1µ
X627 0.1µ
U615C OPA2131J
U616C OPA2277A
U618C TLE2022
STANFORD RESEARCH SYSTEMS, INC.
Title
Precision Current Preamp, Analog Board: Autozeroing Amplifier
Size C
Document Number SIM918
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Date: Thursday, October 05, 2006
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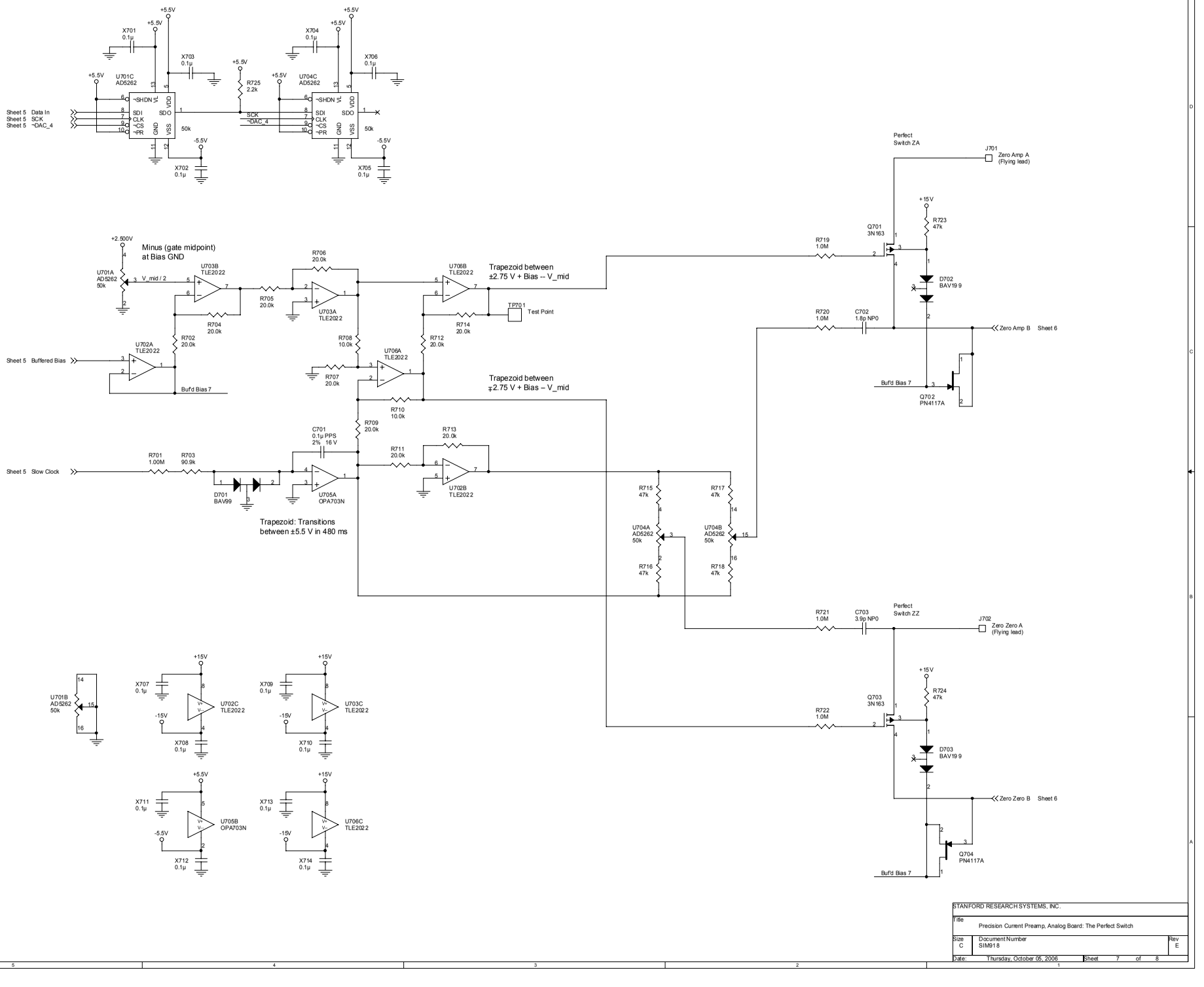

STANFORD RESEARCH SYSTEMS, INC.		
Title: Precision Current Preamp, Analog Board: The Perfect Switch		
Size: C	Document Number: SIM918	Rev: E
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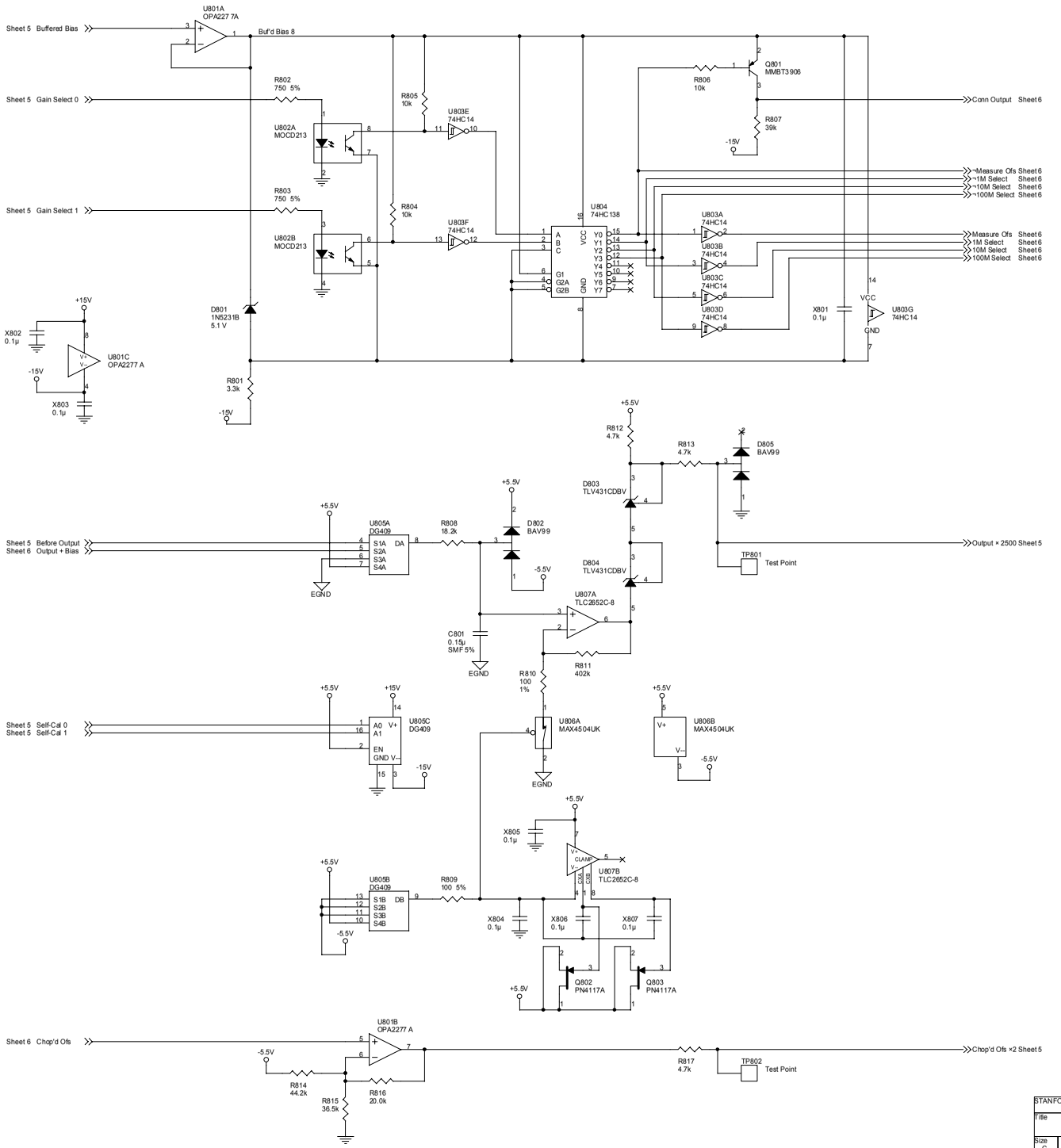

STANFORD RESEARCH SYSTEMS, INC.		
Title: Precision Current Preamp, Analog Board: Gain Switch and Self-Cal		
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Appendix A Index